

analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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Editor's Notes

TEMPUS FUGIT

Unbelievable! These pages complete the 20th year of the under-signed's stewardship of *Analog Dialogue*, the 22nd year of its publication, and the 23rd year of ADI's corporate existence. Since some of our readers may not yet have been born when we took over the helm, it would not seem inappropriate to pause for a few personal reminiscences.



It seems only yesterday that we learned about analog computers at the knee of George A. Philbrick; assisted at the birth of the first commercial differential-input op amp, the K2-W, in 1952; and chronicled many of the great moments of progress in op amps and analog devices—and their applications—in Philbrick publications. Our flagship was called *The Lightning Empiricist* (with a high-speed repetitive analog computer, the solution would change before your eyes as you adjusted a parameter, hence the title).

After Philbrick's merger, the "great moments" seemed few and far between; as a result, Ray Stata's formidable persuasive powers were not heavily taxed to make clear to us where Opportunity lay. Since then, there have been many great moments, most of which have been joyously documented in these pages.

When we arrived in Cambridge on a cold January morning in 1969, ADI was an op-amp specialist on the threshold of becoming a converter manufacturer; our own integrated-circuit fab was a year or two away; microprocessors were in their infancy, the personal computer was very much a dream, and the computer-as-component was a wild idea. So the excitement, over the years, was not only in our own development of products and technologies, but also due to being very much in the mainstream of a rapid but stable growth segment of the electronics industry.

But our readers have been reminded of all this from time to time, so we'll use the rest of this space to discuss a more-pedestrian issue—tools. When we came aboard as engineer-turned-editor, an IBM Selectric permitted rapid typing, but mistakes had to be covered up with a white liquid. The later Correcting Selectric used a roll of sticky tape inside the machine to pick up mistakes; but rearrangement of paragraphs called for scissors and paste.

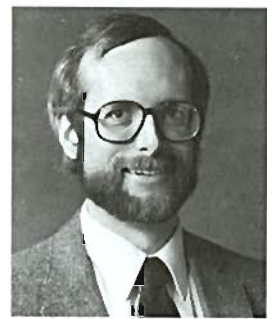
A Wang word-processing system solved those problems; it later became especially useful when we could eliminate the time and errors of re-typing by transmitting documents electronically to a Mergenthaler typesetting system—but Greek letters, math symbols, and formatting still required personal attention.

Now articles are assembled on a Macintosh and transmitted to a Xyvision system, which interprets everything from Greek characters to font, type size and style, and quickly produces high-resolution camera-ready page text. Unfortunately (well, perhaps fortunately for our career), it can't decide what's important for our readers to know, get authors to write articles, understand the technical issues sufficiently to discuss matters of substance with authors, and edit articles with subtlety to make them clear, readable, and as accurate as *humanly* possible. ▣

Dan Sheingold

THE AUTHORS

Chris Mangelsdorf (page 3) designer and project manager for the AD770, is Senior Scientist and a Design Group Leader at Analog Devices Semiconductor's Converter Operating Group, Wilmington, MA. He has MS and PhD degrees in EE from MIT—plus a BS in Physics with high honors from Davidson College, NC. His doctoral thesis was entitled, "A Distributed Bipolar Device for Monolithic A/D Conversion". He enjoys basketball and windsurfing.



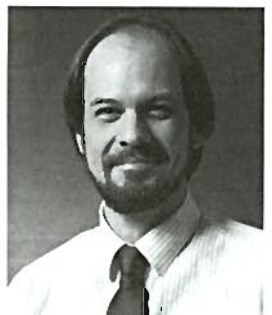
Chris Noble (page 3) is Marketing Manager for Linear Products at Analog Devices Semiconductor; at the time the article was written, he was Product Marketing Manager for A/D Converters. He has been with Analog Devices for five years. He has a BSEE from McGill University, in Montreal, and an MBA from MIT. His hobbies include skiing, sailing, reading, and travel.



Beth Harwood (page 8) is an Applications Engineer in the Analog Devices Component Group, in Wilmington, Massachusetts. She joined Analog Devices upon graduation from the University of New Hampshire with a BSEE in 1986. Her favorite leisure-time activity is skiing; fair-weather interests include golf, tennis, and biking.



Carl Browning (page 8), a Test Engineer in the Converter Group at ADS, is a graduate of Northeastern University. He has AE and BE (with high honors) degrees. He joined the Converter Group from ADI's Component Test Systems Division, where he was a Design Engineer. Earlier he had been a Design Engineer at GCA Corporation and an Associate Engineer at Instrumentation Laboratory, Inc. He enjoys gardening, family, and tinkering about the house.



(More authors on page 30)

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106

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200-MSPS 8-BIT IC A/D CONVERTER HAS 250-MHz BANDWIDTH

AD770's Error-Correcting Circuitry Enhances Performance Bipolar Input Range, Low Input Capacitance Ease Drive Requirements

by Chris Mangelsdorf and Chris Noble

The AD770* monolithic 8-bit a/d converter uses advanced process technology and flash-conversion architecture to convert at 200 megasamples per second (MSPS) with a 250-MHz full-power analog-signal bandwidth. Wide bandwidth makes this ECL-compatible converter ideal for applications such as waveform digitizers, transient recorders, microwave telecommunications, radar, and ATE. In this article, we will discuss the device's architecture and performance—and show why bandwidth beyond the 100-MHz Nyquist frequency is both necessary and desirable.

Besides being optimized for bandwidth and speed, the AD770 can be driven directly from most signal sources, allows stacking of two devices for 9-bit conversions, and corrects invalid conversion results (such as "sparkle" codes) in real time. In contrast to high-speed but relatively low-bandwidth converters available today, the wide bandwidth of the AD770 obviates the need for an external sample/hold circuit with its inherent design tradeoffs, costs, and errors.

AD770 grades are available for 0 to +70°C and -55 to +125°C operation, with optional ± 1 -LSB or ± 0.75 -LSB max non-linearity. Power consumption, using standard +5-V and -5.2-V supplies, is typically 2 watts. Prices begin at \$175 (100s).

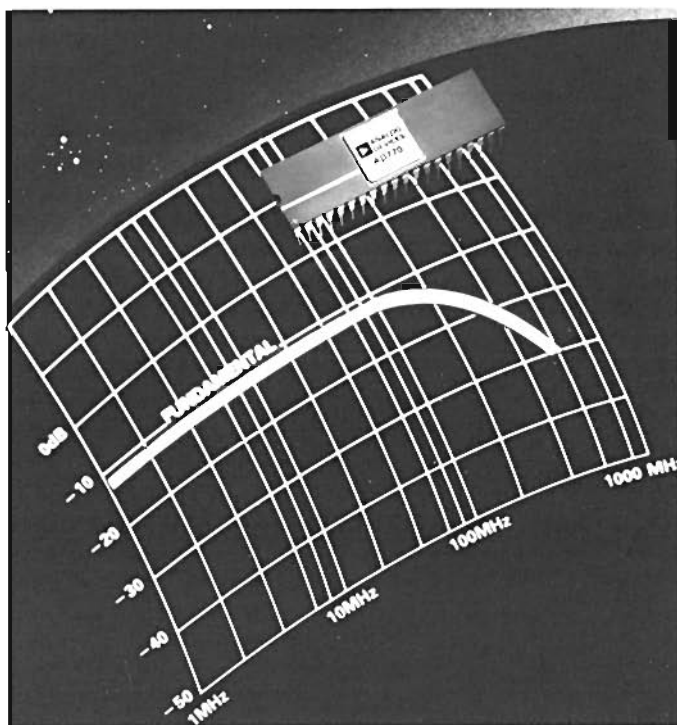
Dynamic performance of the AD770 is fully characterized in the frequency domain for a variety of signal levels and frequencies. Evaluating the performance of such a high-speed device requires careful circuit layout and attention to detail. An evaluation board that incorporates virtually all of the auxiliary circuitry needed is available (see "Evaluation Board Explores Capabilities of AD770," page 8); it includes an optional input buffer, termination resistors, references, digital output drivers, and a reconstruction DAC.

Production-volume testing of a wideband, high-speed ADC with accuracy and speed requires a thorough understanding of what constitutes a valid test, along with insight into limitations of the testing system itself (see "High-Volume Testing of Flash Converters," page 10). A converter that is generating new digital values at 200 megasamples per second produces 1,000 data points in just 5 microseconds, so a major factor in production-testing such a device at adequate speeds is efficient processing of a large volume of raw converter data.

DESIGN OF THE AD770 CONVERTER

As in all flash converters, the architecture of the AD770 is based on a stack of comparators that compare the input with a series of reference voltages derived from a resistor string (Figure 1). For the AD770, each aspect of this basic design was examined for its contribution to performance at the 200-MSPS rate. Timing subtleties, signal-path propagation mismatches, and stray capacitances are significant impediments at that speed.

The converter is fabricated in an ECL-compatible bipolar process employing very small transistors, a major advantage for an 8-bit



converter that requires $2^8 + 1$ comparators (including over- and underrange), with latches and decoding logic to convert the comparator outputs to binary number format. Latches are activated from an external sampling clock, which can be single-ended or differential, with frequency from 0 to 200 MHz.

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The chip design (Figure 2) is symmetrical to equalize propagation delays and stray capacitance. All analog signals connect on one side of the 40-pin package—digital signals on the other side—to rationalize the user's board design so that the final design can realize the VHF potential of the converter. Higher-speed signals are at the center pins to minimize internal lead inductance and capacitance.

Analog Input: The analog input signal simultaneously drives the signal inputs of 257 buffered comparators optimized to combine high speed, low input capacitance, and stability with both temperature and signal amplitude. Inputs can be unipolar or bipolar and up to 4 volts peak-to-peak. Bipolar supplies ensure that signals which exceed the 4-volt spec will cause saturation but no damage to the comparators; overload recovery is fast because of the dual supplies. In contrast, single-supply converter inputs saturate when overloaded by only a few hundred millivolts, with subsequent slow recovery or damage.

High reverse-bias, across the base-collector junctions of the comparator input transistors leads to reduced signal-dependent variations in junction capacitance, thus minimizing a significant source of distortion as well.

These are important features for a converter that digitizes signals with bandwidths above 100 MHz; in the RF regions, many signals (such as radar returns) are not "well-behaved" and can have sudden large changes in amplitude and wide dynamic range, for which even fast automatic gain control (AGC) is not sufficient.

Reference Ladder: The other inputs to the comparators are reference voltages derived from a gold-interconnect precision-resistor string. This string (200 Ω total) has taps at mid- and quarter-points; they allow extra RF bypassing (minimizing reference noise) and even permit linearity trimming or piecewise-linear transfer-function modification.

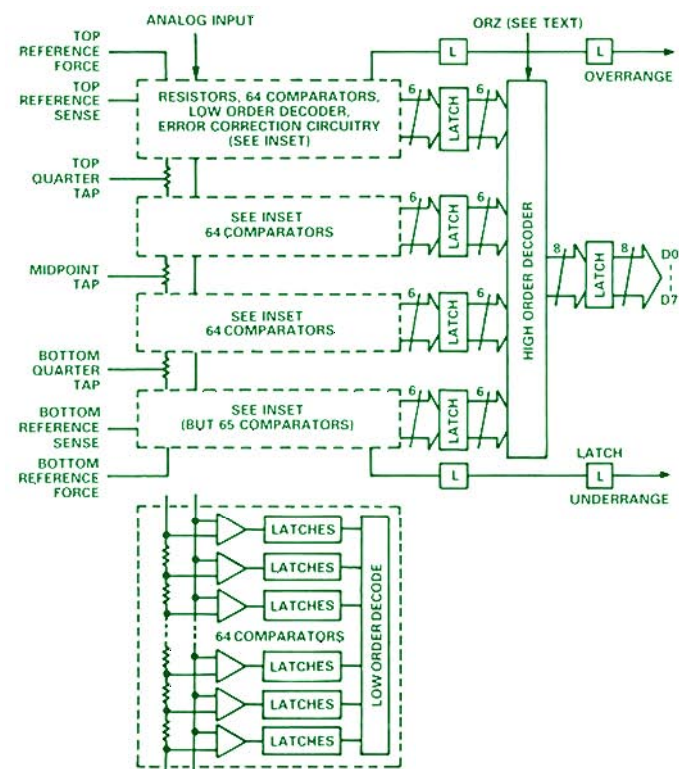


Figure 1. AD770 Block diagram. Inset shows comparator group.

The reference voltages applied to the top and bottom of the resistor string need not be fixed; the AD770 allows the user to supply any values (top more-positive) within a $\pm 2V$ span of ground. For unipolar signals, the reference range is typically 0 to $+2V$ or $-2V$ to $0V$, while bipolar signals—common in RF circuitry—can use a bipolar reference pair (e.g., $\pm 1V$). But the reference voltages *need not be symmetrical*. Further reference accuracy is assured by Force and Sense lines for the reference connections to the resistor string.

The user sets the full-scale range of the A/D converter with the references. The tradeoff depends on the application: sometimes a larger span with better SNR is preferred; in other situations, a smaller span with wider bandwidth is better. At the frequencies at which this converter operates, it is often difficult to get the signal source to slew fast enough to provide large-amplitude inputs to the converter; thus, narrower ranges, such as $\pm 0.5 V$ or $\pm 1 V$, are typical.

Driving the AD770: The 19-pF input capacitance of the AD770 can be driven directly by most signal sources. Input bandwidth, however, is affected by the termination of the signal source, which generally needs to see a 50- Ω impedance. The terminations of Figure 3 both result in 50- Ω low-frequency impedance to ground as seen by the source, but scheme (b) maintains the 50- Ω impedance over a wider range of frequency and provides a lower impedance at the AD770's input over frequency, resulting in a wider -3 -dB bandwidth.

But there is a tradeoff: termination (b) attenuates the input voltage by a factor of two (6 dB); this reduction of signal can be a problem for low-amplitude RF signals. However, the input span on the AD770 can be reduced without losing *digital* resolution if the reference voltage is reduced. Termination (b) makes the source look like a lower impedance to the converter, more than doubling the input bandwidth and fulfilling the bandwidth potential of the converter.

Conversion Logic: The 257 comparators are divided into four groups of 64 (plus an additional comparator in the least-significant group to detect underrange). When the comparator outputs are latched, they drive "low-order decoders" which produce a 6-bit code for the group from the original 64 comparator outputs. These bits, in the highest group with turned-on bits, correspond to the six LSBs of the final 8-bit result. Along with this low-order

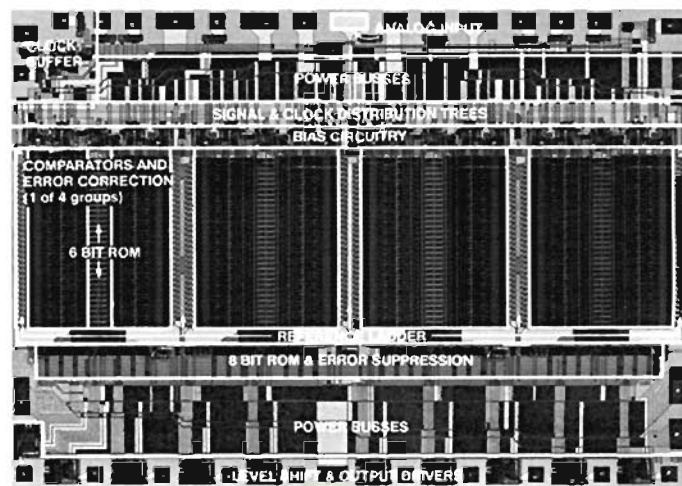


Figure 2. Photo of die, with key functional areas.

decoding is proprietary error-correction circuitry (see box on page 7), unique to the AD770.

Digital Outputs: The four latched groups of low-order results are decoded with respect to one another to produce the two high-order bits of the 8-bit result. All eight bits are then latched and presented as parallel ECL-compatible signals to the user's output bus at a rate of up to 1 byte per 5 nanoseconds.

A unique feature of the AD770 is the presence of both *overrange* and *underrange* output bits; they indicate when an output signal falls outside the reference span (above the top and/or below the bottom reference). They can be used to control the AGC stages in an r-f front end or a programmable-gain amplifier in data acquisition systems. Because they are ECL, they can be wired directly together (wire-OR'd) to serve as a DATA VALID flag, to accompany each data byte through subsequent processing.

Two AD770 converters can be "stacked" to produce a 9-bit conversion by wire-ORing the output data bits of both devices (see page 9). The ORZ (Ovrerrange Zero) input controls the condition of the data bits when an overrange occurs: if ORZ is low, the data bits assume the normal condition of all-ones; if ORZ is held high, the outputs will be zero.

AD770 PERFORMANCE

The design of the AD770 is optimized for bandwidth and speed. Full-power bandwidth, for a $\pm 1\text{-V}$ input, is 250 MHz, while small-signal bandwidth is 400 MHz. The wide bandwidth results in very low harmonic distortion (Figure 4), with response essentially flat to the 100-MHz Nyquist frequency. Signal-to-noise (actually, $-10\text{-noise} + \text{distortion}$, or *signal-to-error*) can be characterized in dB or as effective number of bits (ENOB); $\text{ENOB} = (\text{SNR} - 1.8)/6.02$ for sine-wave input. Figure 5 shows SNR and ENOB versus frequency. For a $\pm 1\text{-V}$ signal at 10 MHz, the SNR is 43.5 dB (6.9 bits), while a $\pm 0.5\text{-V}$ full-scale signal at the same frequency has a 39.5-dB SNR (6.3 bits).

Halving the input range from $\pm 1\text{V}$ to $\pm 0.5\text{V}$ reduces ENOB at low frequencies, since input offsets of the comparators are fixed even though the size of an LSB decreases, thus DNL increases. Interestingly, SNR is better for the lower range at higher frequencies due to reduced slew-rate demands: reduced full-scale range produces a loss of performance at low frequencies but a relative *gain* at high frequencies.

Spectral components of the digital output of the converter can be calculated by using fast Fourier transforms. The result of a 1,024-point FFT analysis of 200-MSPS sampling and conversion on a 95-MHz sinusoidal signal (just under the Nyquist frequency) is shown in Figure 6. Clearly seen are the input-frequency component (0 dB) and a 10-MHz component at -30 dB , the alias of the 2nd harmonic's mirror image (i.e., $-190 + 200\text{ MHz}$); the next largest is -40 dB at most.

It is important that the latches acquire their new state with precise timing. Sampling theory assumes that the samples occur at known, precise time points (which are usually expected to be equally spaced). Sample-to-sample deviations from the assumed sampling times (called *aperture jitter*) look just like input signal noise when the digital outputs are processed with Fourier analysis and discrete Fourier transforms. The typical 3-ps aperture jitter of the AD770 is less than 0.06% of the 5-ns minimum conversion time; thus it has little effect on SNR.

The wide bandwidth of the AD770 means that its input characteristics can be interpreted with RF techniques such as the *Smith chart*. When measured on a network analyzer and plotted, the impedance is seen as consisting of a near-infinite resistance in parallel with a capacitive reactance (the 19-pF input capacitance), which becomes a significant load only above about 200 MHz. This minimizes drive signal requirements on the signal source and loading on the impedance-matching network.

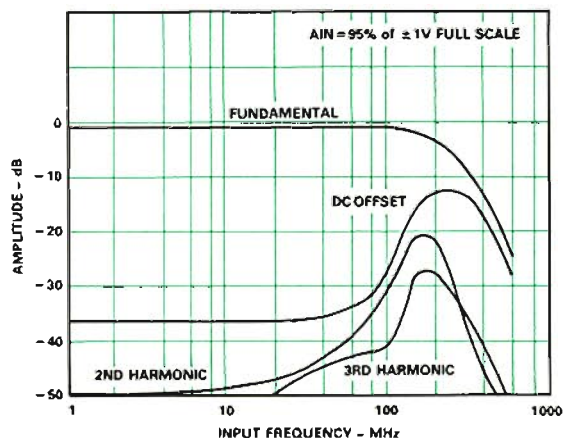
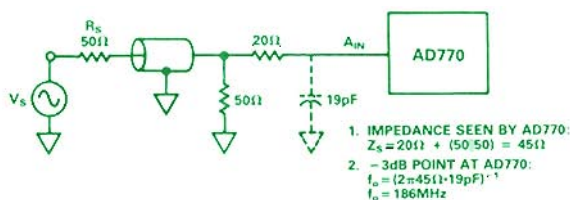
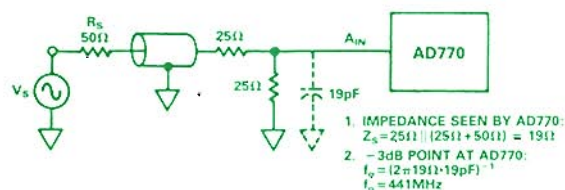


Figure 4. Total harmonic distortion vs. input frequency at 200 MSPS.



a. 50- Ω shunt termination.



b. 50- Ω Termination (-6dB) with 25- Ω series and 25- Ω shunt resistors.

Figure 3. Input terminations and analysis.

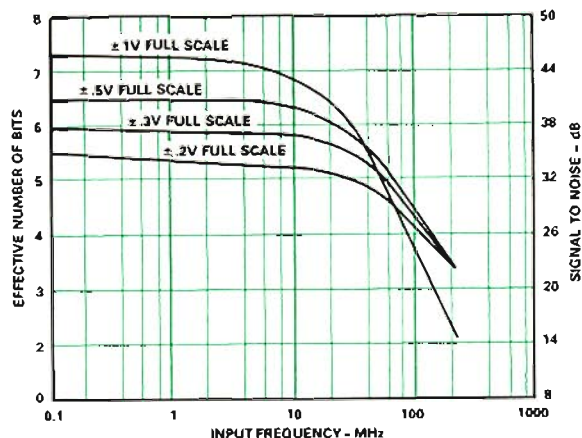


Figure 5. SNR and effective number of bits vs. input frequency, for several full-scale values.

WHEN IS WIDE BANDWIDTH NEEDED?

Most of us are used to systems where the input frequency is restricted to less than one-half the sampling rate, i.e., the *Nyquist frequency*. If that's the basic requirement for capturing completely all the information contained in the waveform, and the AD770's sampling-rate spec is 200 MSPS, with a Nyquist frequency of 100 MHz, why is usable bandwidth of 250 MHz (well beyond the Nyquist frequency) desirable? Wide analog bandwidth of the AD770 gives three benefits: better sub-Nyquist performance, better step response, and usefulness in intentionally aliased applications.

Sub-Nyquist Performance: The AD770's bandwidth is defined as the input frequency (sinusoidal waveform) at which the fundamental component in the reconstructed output has fallen by 3 dB (50% power) relative to its low-frequency value. At this frequency, the amplitude of a sine wave is reduced by about 30%. Using a single-pole model for this phenomenon, the maximum signal frequency for amplitude accuracy at the 8-bit level would be at least one-tenth of the -3 -dB frequency. That's why it is desirable to have the -3 -dB point well beyond the Nyquist frequency, even if the input frequency never gets that high (e.g., when an antialiasing filter with steep rolloff is used).

Step Response: High-speed converters are often used in conjunction with sample-and-hold (SHA) and multiplexer circuits, particularly in instrument applications. This means that the ADC is presented with a sequence of voltage steps as the SHA continually acquires a new sample of the input and holds it for conversion, or as the MUX steps to a new channel. To keep the sample rate high, the ADC must quickly catch up to each new input value. Thus the ADC must have a fast step response, which is equivalent to demanding a wide input bandwidth.

Intentional Aliasing: There are many instances where the familiar injunction against exceeding the Nyquist frequency can be ignored. Two common examples are: the sampling of fast, repetitive signals for oscilloscopic display on slower time bases and the digital detection of modulated high-frequency carriers.

Sampling Oscilloscopes: The concept of a sampling voltmeter (and now oscilloscope) has been used for many years to capture signals with much higher frequencies than the scope can directly display. In a typical sampling scheme (Figure 7), the repetitive waveform of fundamental period, T , (frequency $1/T$) is sampled every

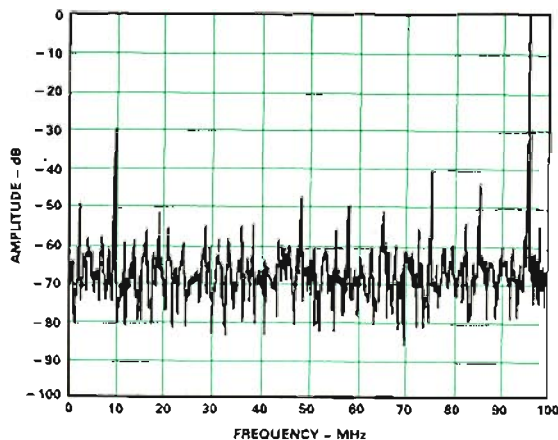


Figure 6. FFT of output for a 95-MHz signal at 200 MSPS. -30 -dB line at 10 MHz is alias of 2nd harmonic's mirror image.

$T + \Delta T$ seconds. The sampled values, overlaid and displayed in sequence, and spaced by ΔT , accurately depict the original signal. (This scheme is sequential, but random sampling order, followed by re-ordering, can also be used.)

The sampling rate is only a fraction of the highest frequency of the signal (which is well beyond the Nyquist frequency), but the converter must be able to pass the signal without attenuating its high-frequency components. Otherwise, the signal's magnitude and shape will be distorted. This approach is called *undersampling*, i.e., sampling at a rate below the Nyquist rate.

When the sampling rate, $1/t_s$, is less than that dictated by the Nyquist theorem, the sampled signal's spectrum contains aliases, where spectral components greater than one-half the sampling rate create difference-frequency components that are "folded" into lower-frequency areas. The aliases occur at [signal frequencies above $f/2$] minus [the sampling rate—and each of its multiples]. Information is lost in the corrupted result. Thus the usual Nyquist rule is simply a warning that frequencies above half the sampling rate may be confused (aliased) with signals of lower frequency.

At first glance, sampling theory thus seems to assume that the entire signal spectrum, from 0 Hz to the Nyquist frequency, is needed to reconstruct the information of interest. However, this is not the case in many applications. A communications signal contains information in a strictly limited bandwidth (sidebands) around a high-frequency carrier. The carrier frequency is assigned based on spectrum allocations, propagation conditions, and factors that are unrelated to the information in the sidebands.

A naive reading of Nyquist's theorem might imply that ± 10 kHz information sidebands around a 200-MHz carrier can only be recovered by sampling at >400.020 MHz. However, synchronous undersampling makes it possible to recover these sidebands as baseband signals. This undersampling produces aliases and makes it possible, with appropriate ratio of sampling rate to carrier, to select any spectral region, such as the band-limited sidebands of the carrier. For example, if a 200-MHz carrier is sampled at 200 MHz (one-half the Nyquist rate), the first alias will be at 0 (i.e., dc); any sidebands associated with the carrier are returned to baseband.

Consider a carrier at frequency, f_0 , with sidebands (Figure 7a), where the sidebands are narrower than the Nyquist frequency, but f_0 is well beyond it. The goal of *a/d* conversion is to recover the information in the digitized sidebands. Synchronously undersampling in phase with the original carrier mixes the carrier and its sidebands down to baseband (heterodyning), Figure 7b, and digitizes the sidebands. In contrast to the simplistic view that undersampling creates useless aliases, the sideband signal is aliased down to baseband, and *this* alias is meaningful.

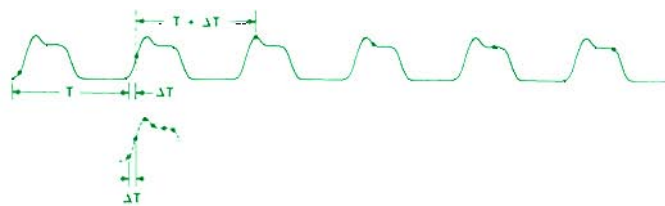


Figure 7. Sampling a high-frequency periodic waveform.

There are two requirements to make this scheme—mixing a high frequency directly down to baseband—work properly. First, the bandwidth of the ADC must be wide enough so that the carrier (and its sidebands) still have sufficient amplitude when they are sampled and converted. The AD770 meets this condition, with a -3 -dB bandwidth at 250 MHz, and useful bandwidth up to approximately 400 MHz (although with fewer effective bits).

Second, the sampling must be synchronized to the carrier. This may seem an unreasonable constraint, but in many applications it is achievable. In some systems, for example, the source and the receiver are at the same location, so the receiver can easily derive the exact frequency and phase of the carrier. Alternatively, the carrier can be recovered from the received signal with a phase-locked loop and used to synchronize the ADC's clock. The synchronous sampling is equivalent to multiplication of a carrier-plus-sidebands by a coherent local carrier, which is done in direct-conversion receiver architectures.

Figure 9 shows a demonstration system used to recover a 10-kHz triangular waveform that amplitude-modulates a 400-MHz carrier (total information bandwidth—first 4 positive and negative harmonics: 1, 3, 5, 7—is 140 kHz). The modulated carrier—which could come from the first IF-stage output in a multiple conversion superheterodyne system—is fed directly to the input of the AD770, set to a ± 250 mV range, to minimize slew-induced distortion. A 200-MHz clock source for the converter is produced by a second generator, which is phase-locked to the carrier generator. The undersampling of the modulated carrier produces aliases, one of which is at baseband (400-MHz carrier $- 2 \times 200$ -MHz sampling rate).

Data bytes that result from the AD770 conversions represent the binary value of the modulating triangular waveform at each sampled time point. This is dramatically seen by using the a/d converter digital output to drive an 8-bit DAC which reconstructs the original triangle, now demodulated and at baseband, as an analog waveform. In effect, the carrier has been undersampled, but its modulating envelope—the 10 kHz triangle—has been over-sampled (sampled at greater than the Nyquist criterion requires) and fully recovered.

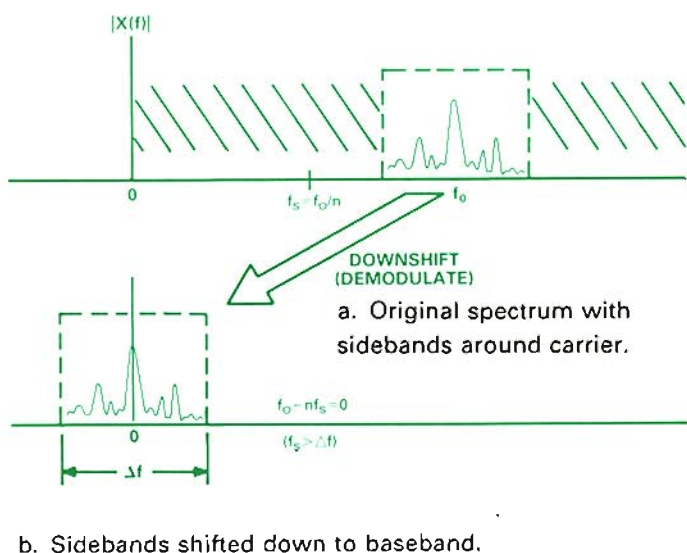


Figure 8. Detection.

In high-data-rate telecommunications systems, the encoded (for error-resistance) digital signal bandwidth is fairly high, as much as 20 MHz. Recovering the modulated data to perform the necessary decoding usually requires complex in-phase/quadrature demodulation circuitry. However, the wide bandwidth and high SNR of the AD770 (32 to 43 dB at 20 MHz; 33 to 40 dB at 10 MHz, depending on amplitude) allows the converter to digitize the signal directly after it is heterodyned down to baseband by conventional techniques. *A priori* knowledge of the coding scheme allows use of optimized algorithms to process the digitized data, recreate the original unencoded bit pattern, and then perform operations such as echo cancellation or adaptive filtering.

FLASH-CONVERTER DYNAMIC ERRORS

Large flash-converter errors can arise from *metastability* and *timing mismatches*. When clocked at high speeds, a comparator has a very short time to decide if the input voltage is above or below its reference voltage. If the input is close to the reference, a comparator may be *metastable* and fail to create a valid logic level within the allotted time. When this invalid signal is passed to the decoding circuitry, the response is unpredictable and leads to output errors. The AD770 latches are designed to maximize converter resolving power and reduce metastability errors to a negligible level.

Slew-rate-induced *timing mismatches* in signal distribution, or comparator speed differences, may cause one comparator to strobe at a slightly different time than its neighbors. Some comparators, in effect, are looking at a different point on the input waveform when the clock signal initiates a conversion. This has no effect for a dc input, but for rapidly changing inputs small timing errors can mean substantial voltage errors, as different portions of the circuitry attempt to generate conflicting output codes. When this happens in the vicinity of major carry points, such as mid-scale, output glitches occur (sometimes called “sparkle codes” because of their visual effect in output-input crossplots and digital video).

The AD770 has two defenses against slew-rate errors. An extensive error-correction scheme (patent pending) finds any comparator with output differing from its neighbors’ and revises its decision, ensuring that a group of comparators must concur on the generation of the output code and that a single comparator cannot act independently. A second defense, in the high-order decode, allows only one of the four 6-bit codes to reach the output (avoiding simultaneity dilemmas). If two groups generate different information due to extremely fast-slewing signals, this circuit arbitrates the conflict and thus averts sparkle outputs.

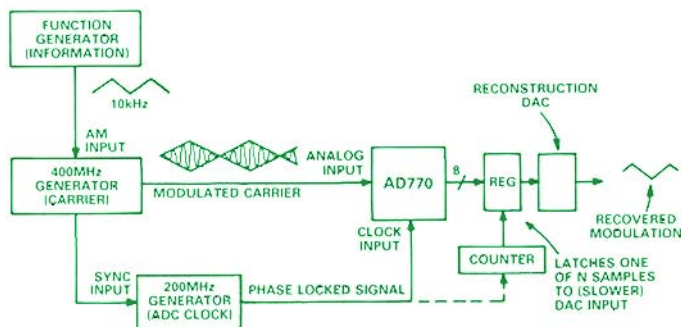


Figure 9. Demonstration of amplitude modulation and signal recovery by synchronous undersampling.

EVALUATION BOARD EXPLORES CAPABILITIES OF 8-BIT AD770

ADEB770 Has Optional Analog Input Buffer, Output Buffers, Adjustable Reference, Decimation, and Reconstruction DAC

by Carl Browning and Beth Harwood

The ADEB770 Evaluation Board* is a tool for users to observe the performance of the AD770 flash ADC at up to maximum speed. Provided is all the support circuitry needed to supply power, proper analog input termination, clock buffering, adjustable voltage references, and ECL-compatible data outputs; operating conditions are selectable by jumpers and resistors. A high-speed DAC reconstructs analog inputs from digitized samples—very useful for observing functionality; and decimation circuitry passes 1-of- N conversions to the digital output buffers when data cannot be accepted at the converter's output rate.

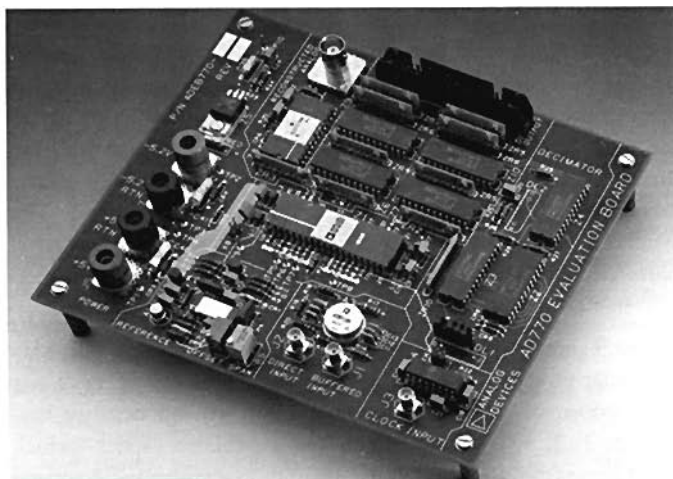
To the user, the evaluation board serves as a quick and relatively painless way to “bring up” a component and exercise its capabilities in the intended application; it also provides a common frame of reference for conferring about observed performance.

FUNCTIONS OF THE EVALUATION BOARD

The ADEB770 (Figure 1) is designed to provide excitation and all input and output signals for the AD770 converter. Due to the high operating frequencies of this device—200 MSPS, 250 MHz full-power bandwidth, 400-MHz small-signal bandwidth—layout and grounding are critical. The multilayer circuit board includes ferrite beads, chip capacitors, inner layers for extensive ground plane and power planes, as well as microstrip transmission lines to maintain necessary impedances at RF frequencies. The converter socket facilitates comparison of performance of different units.

Analog Input: The AD770 can be driven directly via an SMA connector from most 50- Ω sources due to its high and essentially constant input impedance. Loading combinations are available on board to properly match the source impedance in a 50- Ω termination. The series/shunt match provides wider bandwidth but one-half the amplitude of the shunt scheme (see page 5).

For applications that require an input buffer, the analog signal can be routed via an AD9611 transimpedance op amp. Selected after



an extensive evaluation of wideband op amps from Analog Devices and other vendors, this device provides minimal distortion or attenuation of the input over the wide bandwidth of the AD770. Pin-socketed resistors let the user change the closed-loop gain and frequency characteristics of the AD9611 as needed. This is especially useful with low-amplitude RF sources whose limited slew-rate capability precludes prior amplification.

Clock Input: The clock frequency applied to the evaluation board is the conversion rate for the AD770; it can be a sine or square wave of up to 200 MHz. An AD96687 dual high-speed comparator converts the single-ended clock input to a differential ECL signal for the AD770. The clock threshold is jumper-selectable for either ground or ECL threshold, V_{BB} .

Reference Generator: The analog input range of the AD770 is determined by the top and bottom reference voltages applied to the converter and can be anywhere between ± 2 V. Input span is a critical factor in evaluating the AD770's performance: a user may trade a smaller input span, that closely matches the anticipated signal and provides best resolution, for a wider span that has better overrange headroom but poorer resolution and SNR.

Since the range is critical, the AD770 evaluation board provides trimmer-settable independent adjustment of reference span and offset to get the best match between input signal range and the ADC scale. Test points allow the span and offset to be easily monitored. A single AD580 2.5-V reference is buffered and scaled by an AD713 quad op amp, which drives the reference top and bottom inputs via discrete transistors acting as “power buffers”. The buffer outputs to the reference inputs are sensed, and driven to follow the reference-voltage setting accurately, using the 4-wire Kelvin connections of the converter.

Digital Outputs and Decimation: All digital output signals are latched on-board and provided to the external circuitry as 100K ECL signals via a ribbon cable connector, which makes available the 8 data bits (optionally terminated), the clock, overrange, and underrange signals. In addition, decimation circuitry sets the update rate of new data outputs at a selected rate slower than the

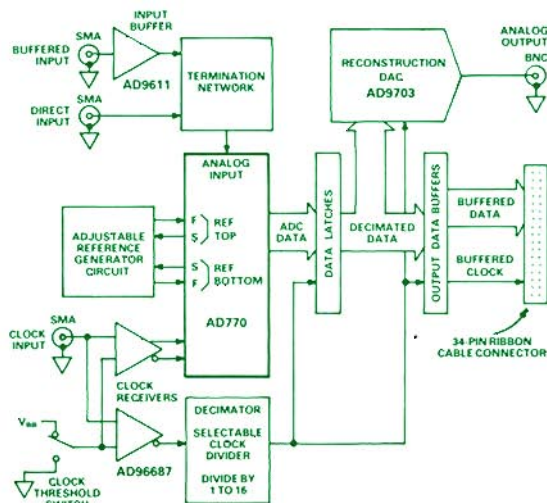


Figure 1. Block diagram.

*Use the reply card for technical data.

actual conversion rate. User-programmed jumpers cause every conversion—or every 2nd, 4th, 8th, or 16th conversion—to be latched at the output.

This sort of decimation is a convenience for users with data-capture systems (e.g., logic analyzers, DFT processors) that cannot accept a new byte every 5 ns, yet who want to exercise the converter at its maximum rate. The algorithms used to analyze the converter's performance need to be modified, because the conversion rate differs from the new data-update rate, but this is still much better than having to evaluate the converter at reduced rates because of instrumentation limitations.

Reconstructed Output: A useful feature of the evaluation circuitry is a reconstruction DAC (AD9703) driven directly by the decimated ADC outputs. The DAC reconstructs the ADC's version of the original analog input signal; the 0 to -1-V output can be monitored on a scope (Figure 2) to provide useful qualitative information quickly about the converter performance. First, it shows whether the converter and evaluation board are working—not a trivial task when the input signal frequency may be greater than 100 MHz and new data outputs are created every 5 ns!

In addition, the DAC qualitatively shows the effects of varying converter operating conditions, such as conversion rate, reference span and offset, and buffering at the signal source. While not intended for parametric measurement—DAC transients and non-linearity errors may exceed ADC errors—the signal reconstruction is the useful equivalent of an analog tuning or trend indicator.

Power supplies for the ADEB770 Evaluation Board are standard: +5 V at 600 mA and -5.2 V at 1.8 A, for ECL compatibility. The evaluation board is available with a choice of ± 1 or ± 0.75 -LSB linearity error (J/K). Prices (single quantity) are \$635/\$725.

Evaluation boards are also available for trying other Analog Devices products, when proper connection of high-performance devices requires careful layout or special connectors to achieve full performance. Typical devices having evaluation boards:*

| | |
|-----------|---|
| AD539 | 60 MHz Analog Multiplier |
| AD1170 | 18-Bit Programmable A/D Converter |
| AD7572 | 5 μ s, 12-bit A/D Converter |
| AD9002 | 8-Bit, 150-MSPS A/D Converter |
| AD9005 | 12-Bit, 10-MSPS A/D Converter |
| AD9012 | 8-Bit, 100-MSPS A/D Converter |
| AD9611 | 280-MHz-Bandwidth Current-Feedback Op Amp |
| AD9615 | 200-MHz-Bandwidth Current-Feedback Op Amp |
| ADSP-2100 | Digital Signal Processor |
| 5BXX | Isolated Signal-Conditioner Series |

*Some are not for sale. Consult ADI sales office for availability.

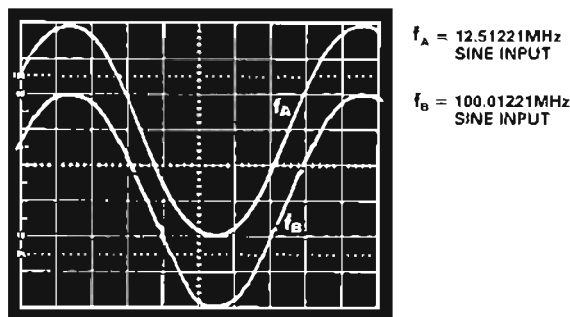


Figure 2. Outputs of reconstruction DAC.

STACKING FOR 9-BIT CONVERSIONS

Two AD770 8-bit converters can be stacked to provide 9-bit conversion at the full rate of the AD770 with no additional logic. The eight data-bit outputs of each AD770 are directly wire-OR'd together (an advantage of ECL), and the lower AD770 is set (via the ORZ control line) to provide "all zero" outputs when over-range occurs. The overrange bit from this converter represents the MSB of the 9-bit data output.

When the input is below half scale, the outputs of the upper converter are zero; when both are OR'd, the outputs of the lower converter provide the actual output bits. As the input increases past half-scale, the lower AD770 overranges, setting the MSB to 1. At the same time, its data output is forced to all-0s. The upper AD770 digitizes the input using its 8 bits to span the upper half of the input range; these digital outputs are OR'd with the 0's of the lower converter to give the eight lower output bits.

The schematic and layout furnished with the ADEB770 evaluation board can be used as a guide to designing a board that accepts two AD770s to perform 9-bit conversions. This can also be realized (more crudely) by adding a "piggyback" adapter for two AD770s to plug into the resident AD770 socket. Since nearly all connections are the same for both converters, this piggyback parallels the IC pins. One exception: the voltage reference string begins at the top of the upper converter, connects its reference bottom to the lower converter's top, and finishes at the lower device's reference bottom—in effect, a single 512-resistor string.

Unfortunately, the reference Force and Sense lines preclude simple series connection of the bottom of one reference to the top of the other. This will short the Force and Sense lines and cause malfunctions. Instead, the reference driver circuitry must be modified, as shown in the simplified schematic of Figure 3.

The upper and lower references—the outer references—are driven as before, via op amp buffers and booster transistors. In addition, two 0.1% resistors between the upper and lower references establish a midpoint reference voltage. This voltage is used as a pseudo-reference for similar circuitry that drives the inner references (upper AD770 reference bottom and lower AD770 reference top) separately, with independent pairs of Force and Sense lines. The divider resistance values are chosen to minimize current drawn from the Sense lines; the buffers must have low offset voltage so that the crossover region between converters is minimized.

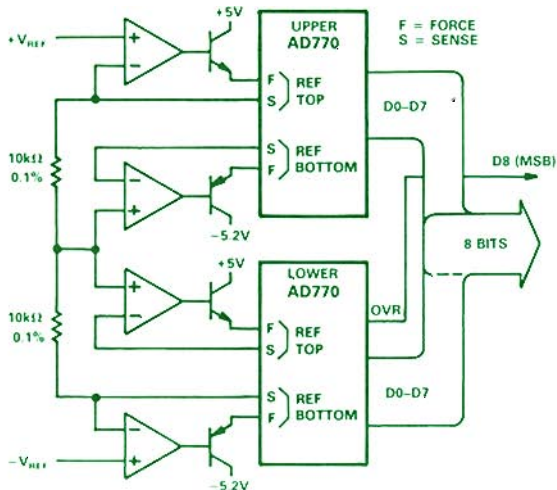


Figure 3. Voltage reference for 9-bit conversion.

HIGH-VOLUME AUTOMATIC TESTING OF IC FLASH CONVERTERS

Verify AD770 Specs with Advanced Mainframe Tester

Special Test Head, Instruments; Copious Software, Statistics

by Rich Johnson

Testing a 200-MHz a/d converter in production volume poses challenges comparable to those encountered in designing and manufacturing it. The ATE system for the AD770 is based on a specially adapted Teradyne A500 mixed-signal tester already in use for testing other products—supplemented with a test head and automatic-device-handler interface of special design, plus additional instrumentation and extensive analysis of the test data. Maintaining signal integrity is difficult yet essential when testing in the high-speed environment for which the AD770 is specified.

Although more than 200 tests are performed (including multiple analyses of single data runs), each part is characterized and graded in less than 20 seconds. Besides product quality assurance and logging, many of these tests are used for better characterization of the AD770 design and processing during the early production phases. Most tests are done with a nominal $\pm 1\text{-V}$ analog input signal, although the converter is also functionally tested at the maximum $\pm 2\text{-V}$ span. Among the many AC and DC tests, key subgroups include speed, linearity, and dynamic performance. Specified for 0 to $+70^\circ\text{C}$ ambient-temperature operation, the device is actually run at 0° , 32° , and 77°C ; the 7° offset, combined with self-heating, replicates thermal equilibrium in the final applications.

The Test Setup: The Teradyne A500 tester, designed for mixed signal (analog/digital) testing, is programmed in a C-language variant running under the UNIX operating system. Many of the standard test- and data-analysis routines provided with this machine were modified or enhanced by custom programming to meet the specific needs of 200-MSPS flash-converter testing. An *immediate window* mode allows the engineer who is developing the test programs to generate and insert program modules without stopping overall system operation. This flexibility is necessary during the product-characterization and test-development stages; but during actual production runs the test program is of course not altered.

The basic A500 was extensively enhanced by Analog Devices' engineers for testing the AD770. The overall test setup, Figure 1, combines the A500 (containing a built-in array processor to speed

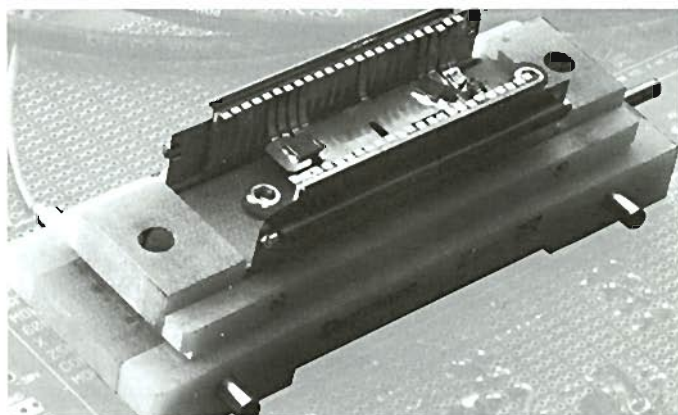


Figure 2. View of special DUT socket fixture.

extensive calculations) with a Sun user workstation, two IEEE-488 bus-controlled sine generators under A500 control, and a test head with the packaged AD770 centered on a handler interface. One generator (with switchable filter network) provides high-purity sine waves of frequencies to beyond 100 MHz for the analog input; the other is a precise clock with rates to 200 MHz and above for AD770 conversions. Signal routing and switching is done with electromechanical relays under program control.

The test head and the handler interface—the device-under-test (DUT) board—are critical parts of the overall system. Each test head has internal analog and digital *channel cards* with the necessary local I/O functions and signal buffering. The analog channel card provides a low-speed analog input source that reaches 10 MHz. Digital channel cards actively terminate and transfer ECL-compatible AD770 outputs to the A500 and provide a low-speed clock (up to 25 MHz) for linearity testing. Another digital card drives the converter input to plus or minus full scale.

The edges of the A500 channel card's low-speed differential clock must occur as nearly simultaneously as possible at the AD770. Signals from this clock are processed by adjustable comparators to correct the timing of the edges with 125-ps resolution. This minimizes transients due to skew between the two clock signals of the differential pair, which would cause the reference ladder bottom to shift—either through coupling or ground transients—and corrupt the linearity tests. While clock signal differential timing errors ideally should have no effect on the reference ladder, the real-world design realities call for compensation.

The AD770 under test is inserted into a specially adapted matched-impedance socket fixture on the DUT board, shown in Figure 2. A "ground sling" suspended between the IC and the fixture contactor assembly is routed out so as to form an extensive ground plane with cutouts for the signal pins. This sling has chip capacitors, which bypass all the dc pins as closely to the IC as possible, and termination resistors for the clock signals. The contactor assembly is located at the center of the circular handler-interface DUT board, which provides local signal-transmission lines and level-shifting, several on/off relays for signal routing,

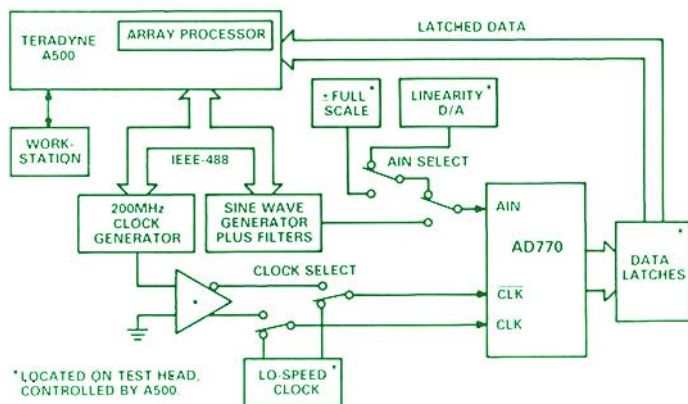


Figure 1. Block Diagram of Test System.

plus additional grounding and chip-capacitor bypassing. Impedances are carefully controlled to minimize mismatch and signal reflections.

Speed: Each AD770 is guaranteed to run at 200 MSPS. Tests are performed at this speed *and at higher rates* to provide a performance guard band and help characterize production lot performance (with a view to yet faster versions). Typical aperture delay and aperture jitter—critical specifications in high speed systems design—are 340 ps and 3 ps rms, respectively.

Linearity: A 12-bit *d/a* converter running at a 2-MHz update rate on an A500 analog channel card—with switching to divide the overall range into four segments to quadruple the DAC's range—is the basis for the linearity test. The DAC output is equivalent to an analog input with 14-bit resolution. A single step of the ramping input DAC represents $2^{-(14-8)} = 2^{-6} = 1/64$ LSB of the AD770 output, so the effective resolution of the actual AD770 code-width in the ramping test can be inferred with great detail.

The digital outputs for nearly 60,000 samples are collected, counted, and represented in a single histogram (Figure 3), which is extensively analyzed. An ideal *a/d* converter would have a perfectly horizontal line all the way across (in this case, at 220) signifying the same number of "hits" at each of the 256 output codes; more hits at any code indicates a wider code span. The histogram data is used to calculate differential and integral non-linearity (DNL and INL). Special algorithms are implemented to compensate for misalignment between the 4 quarters of the 14-bit DAC subsystem, as well as discrepancies at codes 0 and 255.

The histogram can be used to estimate DNL: one LSB is equal to the average number of hits/code for the device, easily gauged by eye. For example, a value of (the average $\approx 50\%$) at any code indicates the DNL for that code is $\pm 1/2$ LSB. The AD770s are graded on DNL, least-squares-best-fit straight-line INL, and absolute-accuracy INL.


Dynamic Performance: Sine-wave signals are the basis of dynamic *a/d* converter tests for this device, as well as many other Analog

Devices converters (*Analog Dialogue* 21-2, page 7) because they are easily generated, measured, and reproduced; they can be described and analyzed fully; and the relationship between sine wave input and corresponding digital outputs is well understood. Frequency-domain testing is based on comparing the actual converter output bits, for a pure sine-wave input, with the digital equivalent of a pure sine wave.

For the AD770, tests are run at the maximum 200-MSPS rate, with sine-wave inputs of 1, 10, 50, and 100 MHz (the Nyquist frequency) at 50% and 100% of FS input. The A500 is programmed to capture every eighth conversion at a 25-MHz rate (due to its digital input speed limitations), using a data-capture clock that is phase locked with the AD770's sampling clock. Subsequent data analysis of the 1,024 acquired data points takes this divide-by-8 decimation into account. At 200 MSPS, data capture takes only 41 μ s ($5 \text{ ns} \times 1,024 \times 8$), an insignificant interval compared to the time required for data analysis.

Captured output data is processed via FFTs to compute signal-to-noise (SNR) and total harmonic distortion (THD). The SNR result is used to compute effective number of bits (ENOB) for the converter, using the standard formula, $\text{ENOB} = (\text{SNR} - 1.8) / 6.02$. A dedicated array processor built into the A500 speeds up the extensive (but very repetitive) calculations.

This A500-based production test system provides large-scale, automatic, and subtle testing. It provides an environment for exercising all of the AD770's functions and ensures that conformance to the data sheet is guaranteed by test. It also gives our process engineers an opportunity to test beyond the data sheet requirements in order to better understand the device fabrication process and its critical variables. In contrast, the ADEB770 evaluation board is the appropriate tool for studying how well the AD770 operates in an intended application, where the electrical environment and the specifications both affect performance.

The high-speed data-capture hardware and associated algorithms were originated by Tim Wilhelm (formerly of Analog Devices Semiconductor); Al Ryan, also of ADS, collaborated on the design. 

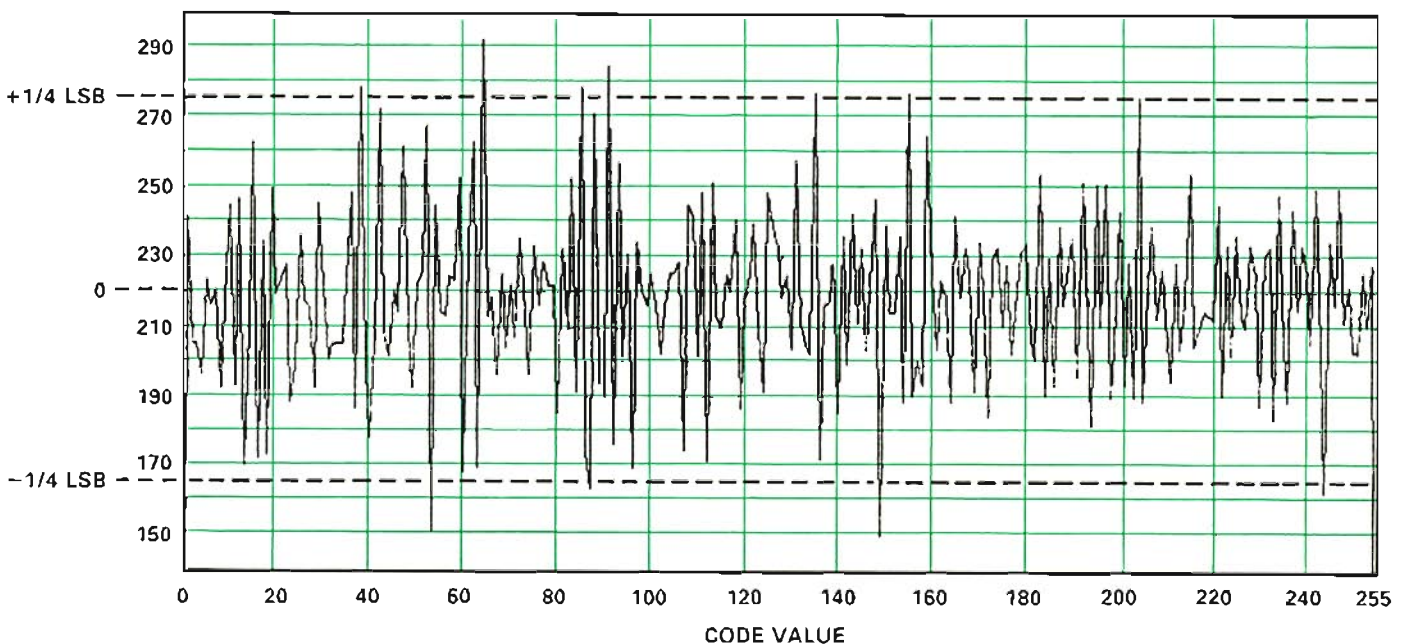


Figure 3. Typical Histogram of Output Codes. Vertical scale indicates number of "hits" and deviation from average, interpreted as linearity error.

OP AMPS COMBINE SUPERB DC PRECISION AND FAST SETTLING

AD840 Series: Complementary-Bipolar Process, Design Expertise, Laser Trim

User Chooses Device Type to Optimize Offset, Bandwidth, Gain, Output Drive

The AD840 series* of op amps provides system, instrument, and equipment designers with an unprecedented combination of dc precision and stability, low noise, wide bandwidth, fast settling, low quiescent power consumption, and substantial output drive capability—in short, an outstanding combination of dc and wide-band performance, the best available to date. All devices in the series, save one, feature settling time of approximately 100 ns to 0.01% for a 10-V step, along with offsets of 1 mV and less. A key factor in the op amps' performance is a complementary bipolar process developed by Analog Devices; it escapes the limitations of conventional linear-IC processes.

We introduce here six devices in the series:

- AD840, stable at gain of $\times 10$, 400-MHz gain-bandwidth product, useful for instrumentation circuits and data acquisition
- AD841, a general purpose buffer with 12-bit accuracy
- AD842, capable of high output-current for high-accuracy line driving
- AD845, a fast-settling FET-input device with high speed and low distortion, can drive 200-pF loads
- AD846, a high-precision transimpedance amplifier with very low static input errors and ac characteristics virtually independent of gain
- AD847, a general-purpose device for <12-bit applications: buffering, driving flash ADCs, and DAC I/V output conversion.

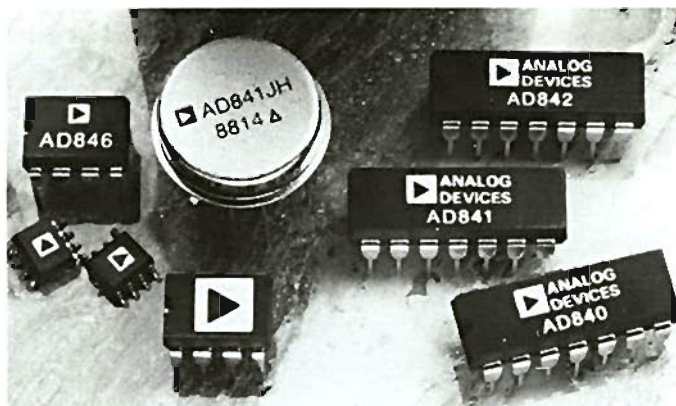
The specifications of devices in the AD840 series are summarized in Table 1. Each is optimized for different application requirements, but many of their general characteristics and capabilities are similar. The benefit to the designer is that in most cases standard parts are now available to meet many of the traditionally conflicting circuit requirements in basically similar applications without external trims or compensation.

THE COMPLEMENTARY-BIPOLAR PROCESS

The complementary-bipolar (CB) process technology of the AD840 series was conceived in the early 1980s, when process, device, and design engineers at Analog Devices decided to see if the inherent limitations on analog designs using existing bipolar processes could be overcome. Some of the goals of this new process were to use standard fabrication-line equipment, process flow, and techniques. However, more process steps could be added if yields could be maintained. Now, as linear device design approaches the 1990s, the AD840 series represents the first fruits of new process and manufacturing technology—key to significantly improved capabilities—applied to overcome a wide range of chronic analog circuit limitations.

In the traditional linear bipolar process, like that used in the industry-standard 711-type op amp, the lateral PNP devices are much slower than the NPN devices. Typical f_T for the PNP device is 10 MHz, while the NPN device has an f_T of 400 MHz.

*Use the reply card to request individual data sheets by model number.



The design of the op amp is optimized for the use of NPN devices, with PNPs used primarily for the output stages. The low f_T of the PNPs limits the op amp bandwidth to approximately 5 MHz.

If we view an op amp as a device whose amplification function is to faithfully steer power from dc supplies to an output under the control of a time-varying bipolar input signal, it is desirable that internal complementary devices be symmetrical for optimum performance. The CB process approaches this with PNP f_T of 700 MHz and NPN f_T at 600 MHz. Not only are these values fairly close to each other (the formerly far-inferior PNP spec is now even slightly greater than the NPN value); both are substantially higher than the former NPN spec. CB is a high-efficiency—high output current, yet low quiescent current—process. Speed no longer means compromises in precision, power consumption, cost, or availability.

The CB process achieves these results by combining ion implantation for up-diffusion along with conventional down-diffusion on a P-epitaxial process (Figure 1). The PNP transistor is made the native device in the structure. Precise construction of the doping profiles—both up and down—reliably puts the desired characteristics into the IC die, with good manufacturing yields. Laser

Table 1. Devices in the AD840 Series and their key characteristics.

| Specification | AD840K | AD841K | AD842K | AD845K | AD846B | AD847J |
|--|-----------------------|--------------|---------------|----------------------|-----------------|--|
| Gain-Bandwidth (MHz) | 400 | 40 | 80 | 16 | 46 | 50 |
| At Min. Stable Gain of | 10 | 1 | 2 | 1 | 1 | 1 |
| Settling Time 10V Step, to 0.01% (ns) | 100 | 110 | 100 | 350 | 110 | 120 (to 0.1%) |
| Slew Rate, $\mu\text{V}/\text{s}$ | 400 | 300 | 375 | 100 | 450 | 300 |
| $V_{OS, \text{max}}$, mV | 0.3 | 1.0 | 1 | 0.25 | 0.075 | 1 |
| $V_{OS, \text{Tempco}}$, $\mu\text{V}/^\circ\text{C}$ | 3 | 35 | 14 | 5 | 3.5 | 15 |
| Quiescent Current (mA) | 12 | 12 | 14 | 12 | 6.5 | 7 |
| Notes | Fast, 12-Bit Accuracy | 50-mA Output | 100-mA Output | FET Input; Cap. Load | Trans-Impedance | $\pm 5\text{-V}$, $\pm 15\text{-V}$ Specified |
| Packages (Plus Plastic DIP, Cerdip) | — | TO-8 | TO-8 | — | TO-99 | SO |
| Price (100s) | \$5.40 | \$7.20 | \$8.35 | \$9.50 | \$7.45 | \$2.95 |

wafer-trimming of precision metal-film resistors, developed and perfected at Analog Devices in the 1970s, is still used where necessary for fine trim.

Because CB is a relatively high-voltage process (36 V), devices can run on supplies of ± 15 V as well as ± 5 V and are specified for both. The same components can be used successfully in both video systems applications (1-V nominal signal levels) and in data-acquisition systems with typical 10-V signals.

Settling time of amplifiers fabricated in CB surpasses that of dielectric-isolation (DI) amplifiers, which achieve their high performance using a well-known—but not totally satisfactory—technique. DI is expensive to fabricate and uses non-conventional processing techniques, often with poor yields. The charge redistribution that occurs in a DI op amp in response to a step input causes a significant and unavoidable settling “tail”, virtually eliminated in CB. The phenomenon can be seen in Figure 2, which shows the error voltage at a dummy summing point.

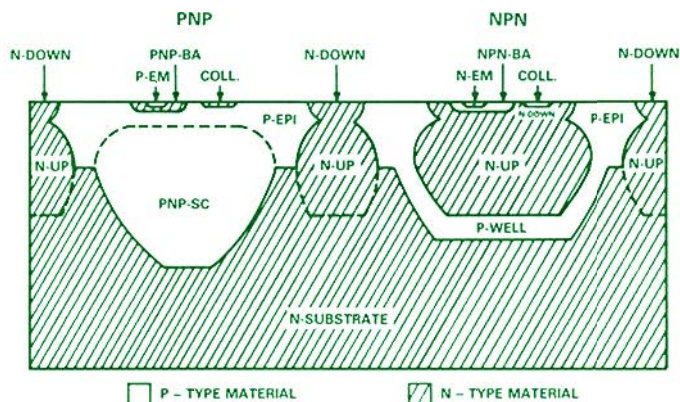


Figure 1. Cross-section of complementary bipolar transistors (BA is base, EM is emitter, DOWN and UP are diffusion directions).

Finally, CB devices are “well-behaved” in application; this is not always the case for op amps using more elaborate design techniques, such as feedforward compensation.

THE AD840 SERIES OF OP AMPS

AD840/841/842: This trio of devices provides wideband, fast-settling performance with accuracy suitable for 12-bit system requirements. The AD840 features a 400-MHz gain-bandwidth product and remains stable over the full operating temperature range for gains of 10 or more. Its fast settling time—100 ns to 0.01% for a 10-V step—and 400 V/ μ s slew rate make it suitable in video and pulse amplifiers, DAC and ADC buffers, as well as instrumentation circuits. Figure 3 shows the settling time versus

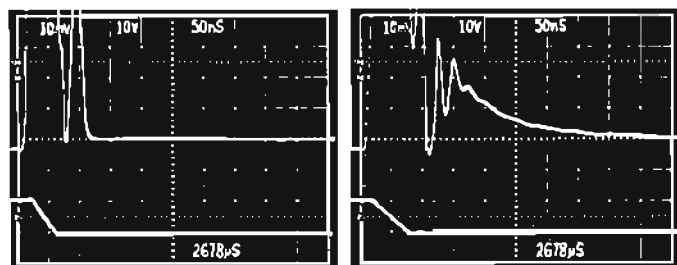


Figure 2. Error voltage comparing the AD841(left) and a DI device showing settling-time “tail”.

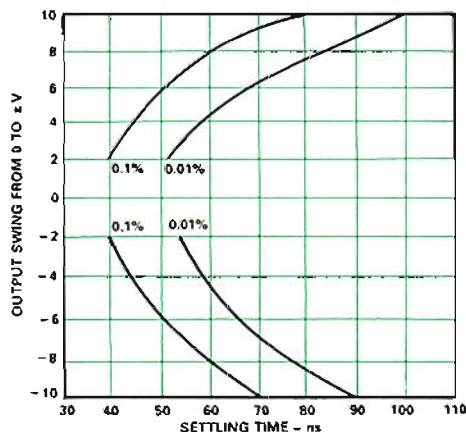


Figure 3. AD840 settling time to 0.1% and 0.01%.

output swing for positive and negative outputs, for 0.1 % and 0.01 % error criteria. Note the symmetrical performance achieved as a result of the CB process.

The AD841 is a unity-gain-stable general-purpose device that serves as an interstage buffer in many applications. It settles to 0.01% in 110 ns, slews at 300 V/ μ s, and has a unity-gain bandwidth of 40 MHz. The AD842 is a gain-of-2-stable device with 80-MHz gain-bandwidth product. Its high, 100-mA output current-drive capability, combined with 100-ns settling to 0.01% (80 ns to 0.1%) for a 10 V step, make it ideal for driving instrumentation and video circuits and low-impedance doubly terminated cables. It also can be used for gains from 2 to 9, more stably than the AD840—with more bandwidth than the AD841.

The AD845 is a fast, precise (12-bit-equivalent), N-channel JFET-input device for active filters, photodiode preamps, and sample-and-hold amplifiers. Unlike many fast amplifiers, which slow down or become unstable when driving capacitive loads, the AD845’s rugged output handles adverse loads with little degradation. The 250- μ V maximum offset voltage eliminates the need for nulling in many applications.

The AD846 provides nearly constant bandwidth and settling time over a wide range of closed-loop gains. Its 12-bit-equivalent (0.01%) performance for ac and dc specifications, along with 450 V/ μ s slew rate, make it useful for residue amplification in multiple-pass ADCs, line driving, audio applications, and video signal buffering. Classified as a *transimpedance* amplifier (voltage out/current in), it is used in much the same way as a conventional op amp; its transimpedance of 500 M Ω results in very high dc precision in op-amp configurations.

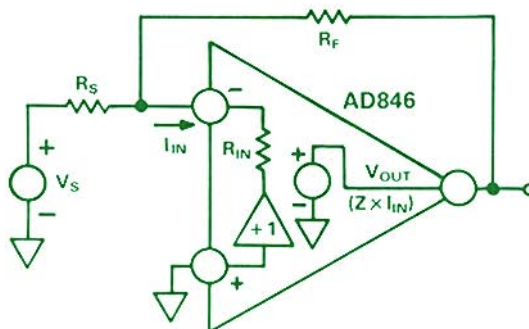


Figure 4. Three-terminal model of the AD846.

Figure 4 shows a three-terminal model of the AD846. The input error signal is developed in the form of a net current out of the summing node, not a voltage. In fact, unlike traditional op amps, which use negative feedback to produce a *voltage null* at the *high-impedance* inverting input terminal, the current-sensing AD846 input terminal has a low impedance (ideally, $0\ \Omega$) to force the node to zero voltage. While the summing action and overall op-amp behavior are generally similar to those of voltage-input op amps, there are significant differences in performance at high frequency.†

For a fixed value of feedback resistance, R_F , the closed-loop bandwidth remains essentially constant, independent of the closed-loop voltage gain. Closed-loop bandwidth as a function of gain for the AD846 is shown in Figure 5 for various values of R_F and compared with a conventional op amp with 46-MHz unity gain bandwidth.

The AD847 features 50-MHz unity-gain bandwidth and a $300\ \text{V}/\mu\text{s}$ slew rate. As a general purpose device, it provides 8- to 10-bit equivalent performance at low cost and low power. The AD847 is internally compensated for unity-gain operation and remains stable while driving any capacitive load. Applications include buffering flash A/D converters, driving video cables, and converting high-speed-DAC current outputs to voltage. Operation is fully specified for both $\pm 15\ \text{V}$ and $\pm 5\ \text{V}$ power supplies to meet the respective needs of data-acquisition and video applications.

Figure 6 shows the output waveform in response to a square-wave input when the AD847, as a follower, drives 100-pF and 1000-pF loads. Although the increased capacitance degrades pulse quality, the op amp does not ring or oscillate.

TESTS AND APPLICATIONS

Measuring Settling Time: Settling time is the interval between the initiation of a step input to a closed-loop amplifier configuration and the time at which the amplifier output enters and remains within a specified error band. Typical bands are 1%, 0.1% (10 bits), and 0.01% (>12 bits). A typical settling-time test circuit for AD840-series op amps is shown in Figure 7.

A fast pulse generator with rise time $<10\ \text{ns}$ drives the op amp. Error voltage is measured by a false-nulling technique which creates a quasi-summing point (*Analog Dialogue* 4-1) that sums

†This action was described for another op amp of this type in *Analog Dialogue* 21-1, p. 22.

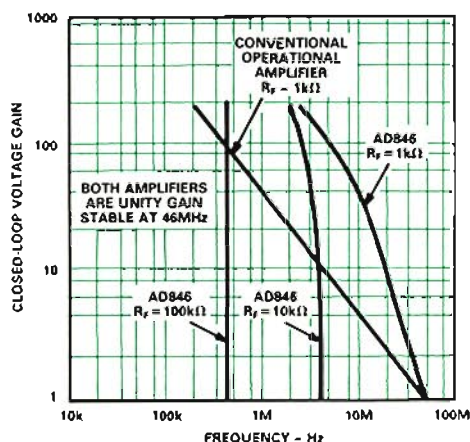


Figure 5. AD846 closed-loop gain vs. bandwidth, for various values of R_F .

positive-going input with negative-going output to measure the error. This simulates the summing point but avoids loading it with probe capacitance. In addition, clamping diodes can be used to prevent the initial error transient from overloading the high-gain measurement input. The scope is clamped to zero until the output enters the error band for the first time.

The results of this test are for the AD845 are shown in Figure 8 for a 0 to $-10\ \text{V}$ step input with a $500\ \Omega || 100\ \text{pF}$ load. The upper trace shows the positive-going AD845 output. Error voltage is shown in the lower trace, at $1\ \text{mV}/\text{div}$. The settling characteristic has four main segments: propagation through the amplifier; slewing time when the output approaches the final value; recovery time from overload associated with the slewing; and linear settling to within a specified error band.

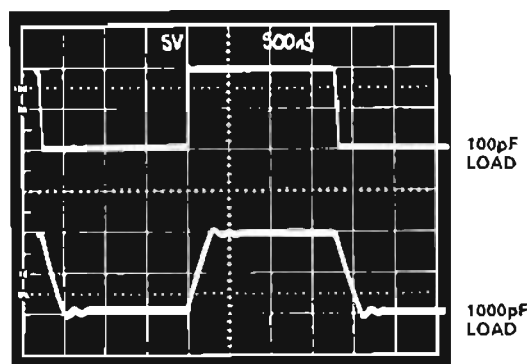


Figure 6. AD847 driving capacitive loads.

Audio Amplifier: The AD846's fast settling and highly linear input characteristics make it an excellent audio amplifier. Figure 9 shows a circuit for a 2-stage phono preamp (RIAA equalized) and line driver. The AD711 op amps, which provide accurate control of dc set points, can be replaced by their double (AD712), or even quad (AD713), versions in multiple-channel applications. Note that the AD846 is used as a follower-with-gain, with the input at the non-inverting terminal. For this reason, the gain can be changed by changing the feedback ratio without affecting either input loading or bandwidth).

Driving the Input of an A/D Converter: An op amp that drives the input of a successive-approximation (SA) converter must provide a constant output voltage while load conditions are changing (Figure 10). In the SA converter, the input current is compared to

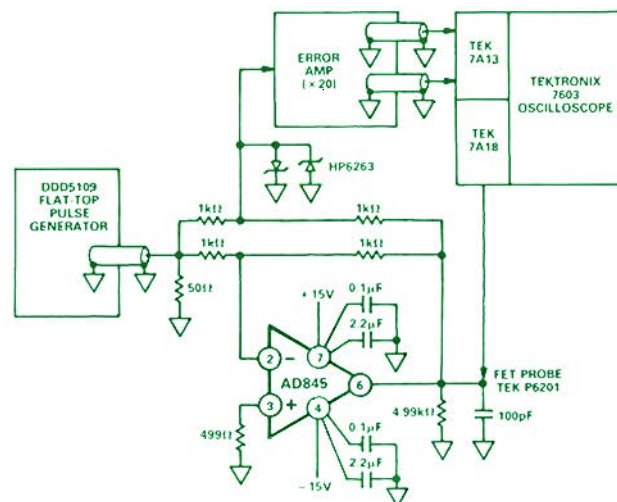


Figure 7. Settling-time test circuit.

a succession of trial currents. Although the comparison node is diode-clamped, it may still deviate by several hundred millivolts, resulting in modulation of the input current at the switching frequency. Output impedance of a feedback op amp is decreased by the loop gain; at higher frequencies the loop gain (especially that of high-dc-precision, narrow-bandwidth op amps) can decrease to the point where the output impedance approaches its open-loop value, typically 25Ω (due to internal current-limiting resistors). A change of a few hundred microamperes in converter loading will cause instantaneous input-voltage errors.

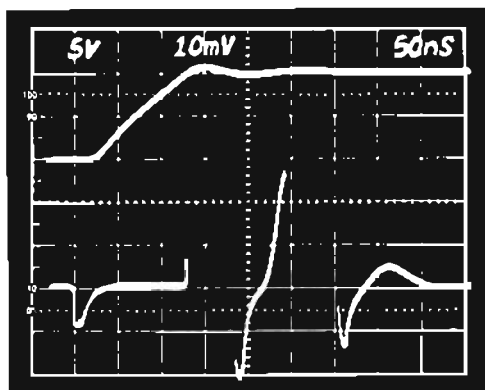


Figure 8. AD845 settling characteristics, 0 to 10 V step.

For slower converters and wide-bandwidth amplifiers, the op amp output recovers to the nominal value before the converter's bit comparison. However, a narrow bandwidth op amp will recover slowly from this transient. The AD845's wide bandwidth and high open loop gain make it suitable for 12-bit converters with conversion times as short as $5 \mu\text{s}$.

Video Line Driver: As a video line driver, the AD842 can drive both terminated and unterminated cables. Figure 11 shows an AD842 as a gain-of-2 follower driving a doubly terminated cable, where termination resistance, R_T , equal to the cable characteristic

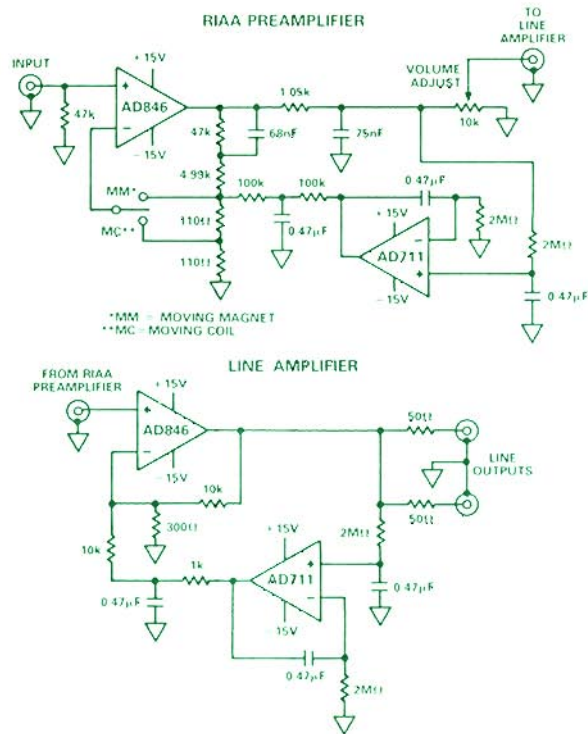


Figure 9. RIAA preamplifier and line driver.

impedance, Z_0 , minimizes reflections from the far end. Back-termination resistance, R_{BT} , also equal to Z_0 , is used between the AD842 output and the cable's near end to damp any reflected signals resulting from mismatch between R_T and Z_0 .

The result is a "cleaner" signal on the video line, but the op amp output must swing $\pm 2 \text{ V}$ in order to achieve $\pm 1 \text{ V}$ at the line, due to the resistive-divider action between R_{BT} and the cable's Z_0 . The AD842, with $\pm 100 \text{ mA}$ minimum of output drive, can supply $\pm 5 \text{ V}$ into a 50Ω cable. Its $375 \text{ V}/\mu\text{s}$ slew rate means that the AD842 can drive a 6-MHz signal to $\pm 10 \text{ V}$, (20 MHz to $\pm 3 \text{ V}$).

If the current-drive requirement is not as high, the AD847 may be used in place of the AD842. Termination is not always needed or possible if signal integrity is sufficient for the application—or grounds have excessive high frequency noise. The capacitive load that results from an unterminated cable—as well as from many other types of loads—is not a problem for the AD847, which is stable for any capacitive load.

Wyn Palmer designed the devices in this series (with Barry Hilton on the AD846). The Analog Devices CB process resulted from collaboration by Fellows Barrie Gilbert, Jody Lapham, and Lew Counts. All of the above are at Analog Devices Semiconductor.

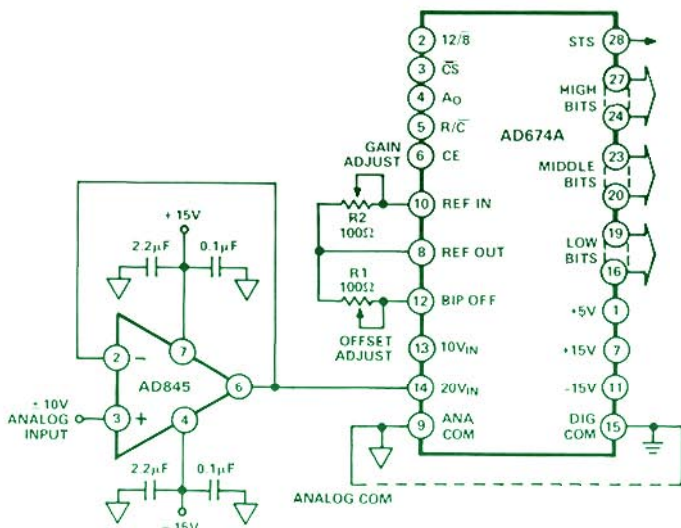


Figure 10. AD845 as a unity-gain ADC buffer.

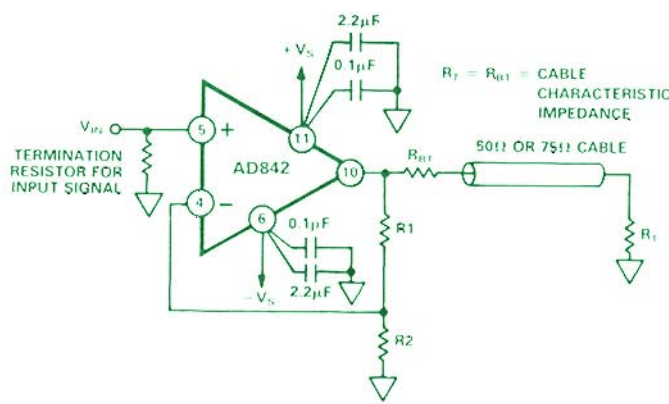


Figure 11. AD842 as terminated line driver.

FOUR-CHANNEL VIDEO MULTIPLEXER SUSTAINS 30-MHz BW

Monolithic AD9300's Switching Rates Exceed 20 MHz

Multiple Devices Can be Cascaded for Larger Matrices

The AD9300 Video Multiplexer* provides 4-to-1 multiplexing of wideband signals with up to $\pm 2\text{-V}$ magnitudes for video and data-acquisition applications. A 2-bit, TTL-compatible Channel-Select code directs one of the four inputs to the single output, switching at rates of 20 MHz and more (depending on signal magnitude). A Chip-Enable control line can force the output to a high-impedance state regardless of the Select code; this allows multiple devices to be configured for larger switching matrices, e.g., 8×1 , 16×1 , 4×2 , 8×2 .

Fabricated in an advanced bipolar process, the AD9300 contains an active buffer amplifier (Figure 1), greatly reducing concerns about the effect of on-resistance of traditional passive switches in routing video-bandwidth signals. This contrasts to existing CMOS/DMOS FET-type multiplexers which form a bidirectional signal path when the switch is closed, with performance-degrading high on-resistance and significant stray capacitance.

For video applications, such as signal routing, imaging, and electro-optics, the key specifications are *crosstalk rejection*, *differential phase and gain* performance, and *overshoot*. Data-acquisition applications emphasize *distortion vs. frequency*, *slew rate*, and *power-supply range*. The monolithic AD9300 provides excellent performance for both applications areas.

Full-power bandwidth is greater than 30 MHz (slew rate of $190 \text{ V}/\mu\text{s}$), with small-signal bandwidth of 350 MHz. Crosstalk rejection of nearly 90 dB at 1 MHz and 75 dB at 10 MHz (one channel grounded and a 2-V p-p signal on the other three channels), minimizes interference from adjacent unselected channels (Figure 2). Gain flat to within $\pm 0.1 \text{ dB}$ up to 8 MHz and differential phase and differential gain errors below 0.05° and 0.05%, respectively, effectively maintain video signal matching between channels. Harmonic distortion, specified for a 1-V peak-to-peak sine wave input and a $2\text{k}\Omega \parallel 10 \text{ pF}$ load, is below -75 dBc to 10 MHz, increasing to -45 dBc at 80 MHz.

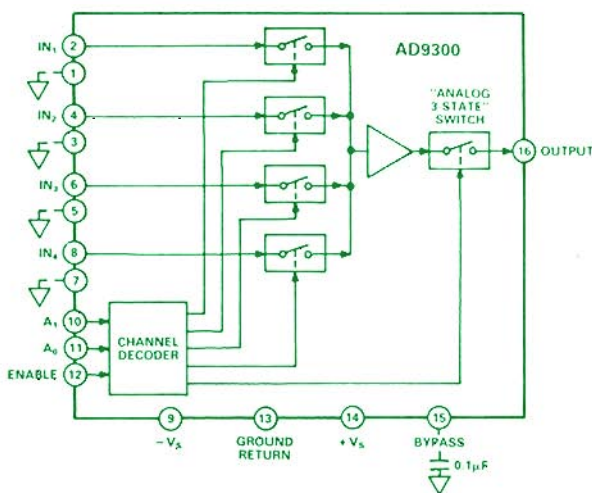
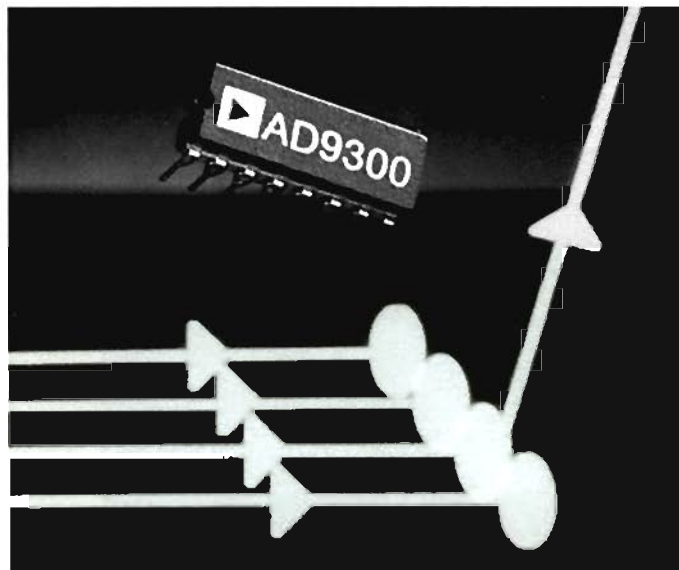


Figure 1. Block diagram.



The T-step response test, traditional in the video industry for measuring overshoot characteristics, uses the rising edge of a $\sin^2(t)$ waveform with 10%-to-90% 125-ns rise time. With a 0 to 700 mV step, overshoot for the AD9300 is less than 0.1%. For a pulse input with slew rate greater than $250 \text{ V}/\mu\text{s}$ the overshoot is less than 10% (Figure 3).

Another aspect of the dynamic performance of the AD9300 is shown by t_{off} , the switching time required for the output to reach a high-impedance state (10%) after the Enable line goes to the inactive state (50% point). Figure 4 shows that this is dependent on the output load resistance; t_{off} is 30 ns maximum for a $1\text{k}\Omega$ load; it increases with the load resistance. Capacitive loads $>10 \text{ pF}$ limit the full-power bandwidth and increase t_{off} .

Cascade and Parallel Configurations: The Enable control line, high-impedance inputs, and high-impedance output when disabled, allow multiple AD9300s to be combined into switching matrices, needed for signal-routing systems and radar systems. Simple paralleling of additional AD9300s handles additional inputs; outputs of multiple devices can be connected together, as long as only one device is selected—only $1 \mu\text{A}$ of bias

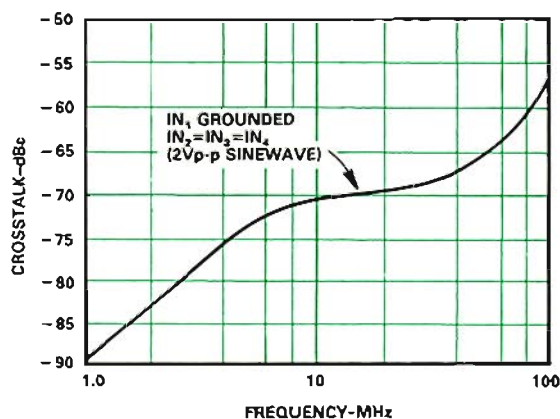


Figure 2. Crosstalk versus frequency.

*Use the reply card for technical data.

current is drawn from the multiplexer output load. Multiple device configurations with *input* signals connected to more than one AD9300 form an $m \times n$ switching matrix, where m is the number of unique inputs and n is the number of output ports.

Figure 5a shows an 8×2 matrix, which allows any of eight signals to be switched to either of two outputs. Three data lines, D0–D2, steer one of the eight inputs to Output 1; three additional lines, D3–D5, choose the input for Output 2. When the outputs of multiplexers #1 and #2 are connected to Output 1, only one device can be active at any time. Similarly, the outputs of multiplexers #3 and #4 provide Output 2. The truth table (b) demonstrates output independence; the same, or different, inputs can be steered to both outputs simultaneously.

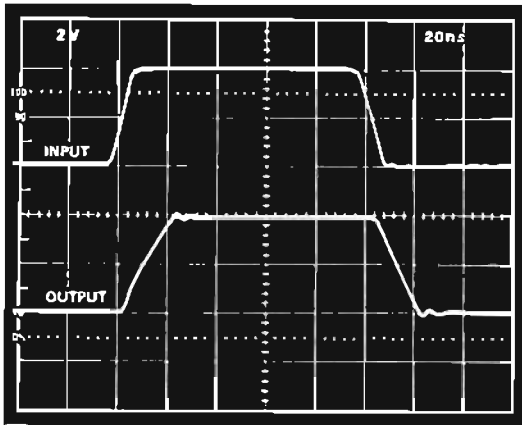


Figure 3. Response and overshoot for a 250-V/ μ s pulse.

Chroma-key applications: The pictures from two standard video cameras can be merged, with one as the apparent background image for the other, by chroma-keying. In video productions, this technique creates scenes that are impossible or impractical to generate in a studio, such as a beach scene. In chroma-keying (Figure 6), the combined video signal is switched between background and foreground cameras during each raster scan, based on information in the foreground video signal itself. A uniform, unique color not occurring in the foreground subject, such as dark blue, is used as the foreground camera's backdrop.

Both cameras are driven from the same master clock for synchronization, and a comparator continuously checks the signal level from the blue vidicon of the foreground camera. When this signal

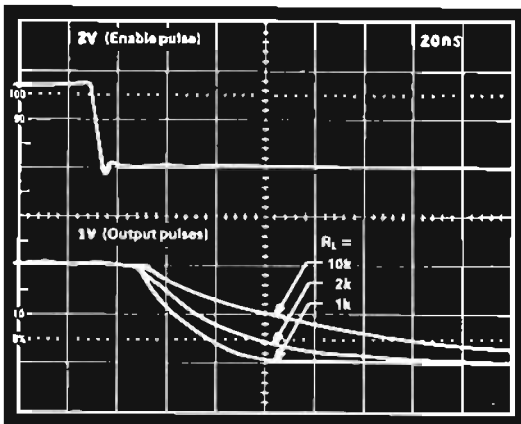
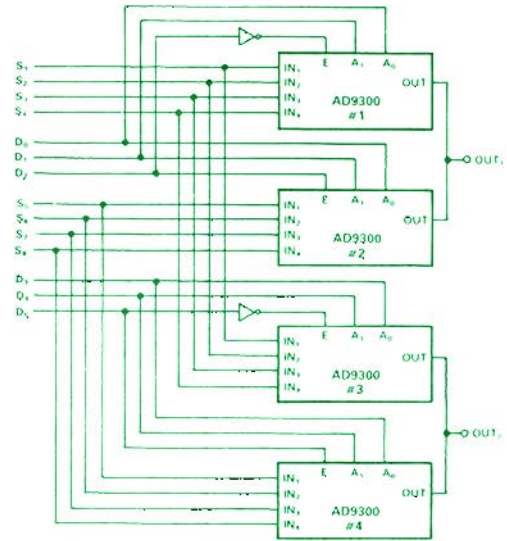


Figure 4. Chip-enable to channel "Off" response time as a function of R_L .

indicates the dark blue (i.e., backdrop) is present, the comparator switches the composite output signal to the background scene camera. When there is no dark blue, the foreground camera signal is the composite output.



a. 8×2 switch matrix with 4 AD9300s.

| D_2 | D_1 | D_0 | \Rightarrow | OUT_1 |
|-------|-------|-------|---------------|---------|
| D_5 | D_4 | D_3 | \Rightarrow | OUT_2 |
| 0 | 0 | 0 | | S_1 |
| 0 | 0 | 1 | | S_2 |
| 0 | 1 | 0 | | S_3 |
| 0 | 1 | 1 | | S_4 |
| 1 | 0 | 1 | | S_5 |
| 1 | 1 | 0 | | S_7 |
| 1 | 1 | 1 | | S_8 |

b. Truth table for 8×2 matrix.

Figure 5. Switching matrix application.

Standard NTSC color video cameras produce signals with about 6-MHz bandwidth—easily handled by the AD9300's bandwidth and gain flatness—the equivalent of 384 pixels/line in a 63.5- μ s line, or a new pixel every 165 ns. This means that the chroma-key multiplexer must switch in 165 ns for abrupt pixel-by-pixel changes. The AD9300 speed for "digital code to channel output on or off" state—under 50 ns—is faster than needed. Cameras for use with computers, and those compatible with PAL and SECAM systems, have slightly higher pixel/line values and line rates but are still easily within the multiplexer's capability.

An on-board bias network makes the performance of the AD9300 independent of the supply voltages, which can be between ± 10 V and ± 15 V dc. The AD9300 is available in 16-pin cerdip for 0–70°C and –55 to +125°C ranges, with a 20-pin LCC also available for the mil-temp range. Prices begin at \$8 (100s).

The AD9300 was designed by Dana Zipperer at the Analog Devices Computer Labs Division in Greensboro, North Carolina. ■

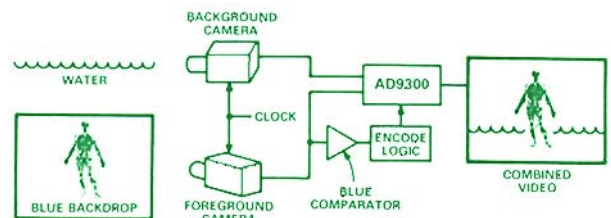


Figure 6. Block diagram of chroma-keying application.

3 ANALOG AND DIGITAL I/O BOARDS FOR THE PS/2 MICRO CHANNEL

12-Bit Analog/8-Digital I/O: RTI-204 & 205; 32-Bit Digital: RTI-217

Have High Functionality, Software in 6 Languages, Meet PS/2 Specs

by Peter E. Predella

THE MICRO CHANNEL

If more and more process-controlled laboratories and factories replace their PC-based data-acquisition systems with the IBM Personal System/2, there are good reasons. The PS/2 incorporates an advanced 32-bit bus architecture, called the "Micro Channel", capable of performing 40 to 150% faster than that of the IBM PC/AT. A 32-bit data path and Micro Channel's arbitration scheme—allowing several coprocessors to control the bus simultaneously—provides speedy data access and transfer.

PS/2's surface-mount technology reduces power consumption and chassis size and increases component life. Because board manufacturers recognize that IBM PS/2 can solve future problems of networking, connectivity, communications and multitasking, Micro Channel-compatible I/O boards are appearing in increasing numbers.

WHAT DOES THE PS/2 OFFER DATA ACQUISITION?

The PS/2's design attacks two common problems related to the data acquisition of real-world phenomena (e.g., temperature, pressure, speed, motion, flow and light). The first is noise and interference caused by power supplies and high-speed switching, both inherent in PCs. The PS/2 uses interspersed ground and power lines to reduce internal electronic interference. A ground line within 0.1 inch of each Micro Channel signal line provides shielding and guarding—diminishing stray coupling. This well-thought-out architecture enhances the ability of data-acquisition analog and digital I/O boards to accept and produce cleaner, more reliable signals.

Another improvement over the PC is the PS/2's ability to enable or disable the read/write capability of an adapter board. The PS/2 periodically checks board outputs and compares them to a permissible range. Values outside the range cause the anomalous result to be ignored and the program to continue cycling. In effect, I/O boards with anomalous results will not "hang-up" a system due to an unexecutable "read". The result—a fault-tolerant data-acquisition and control system.



Select to avoid future dilemma. The system is designed to function optimally with boards that comply with its personality requirements. Thus, besides seeking specified functional performance to solve a given task, designers of data-acquisition systems should consider I/O cards that fully comply to IBM PS/2 specifications, i.e., boards with software-programmed interconnections free of DIP switches and jumpers. Selecting only boards meeting these criteria will cause the system to tend to run at optimum speeds with minimal errors.

HIGH-FUNCTIONALITY I/O CARDS

Analog Devices manufactures three high-functionality Micro Channel-compatible analog and digital I/O adapter cards that operate in PS/2 (models) 50, 60, 70 and 80. The RTI-204,* RTI-205,* and RTI-217* are designed for researchers and industrial system designers looking for a versatile and cost-effective method of monitoring, controlling and data-logging environmental events with little need for attention to interfacing the measurement circuitry to the system hardware and software. All three boards use Analog Devices' proprietary bus-interface chip for timely access to and transfer of data; and they all conform to PS/2's many specifications for interface boards.

Data Acquisition input. The RTI-204* (Figure 1) is a low-cost analog input and digital I/O board. It accepts eight single-ended analog inputs, converts them with 12-bit resolution at rates up to 19 kHz; the conversions can be short-cycled under software control to 8-bit resolution for increased throughput rates up to

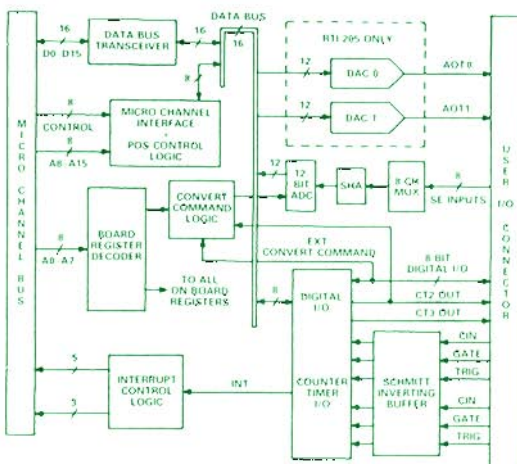


Figure 1. Block diagram of the RTI-204/205.

*Use the reply card for technical data.

QUAD PRECISION BiFET OP AMP HAS SUPERIOR AC AND DC SPECS

AD713 Is a Multiple of Single (AD711) and Dual (AD712) Versions

Retains High Performance, Adds Monolithic-Match Characteristics

The AD713* comprises four fast-settling-and-slewing, wide-bandwidth AD711-type BiFET op amps with excellent dc characteristics (*Analog Dialogue* 20-2) on a single IC chip. Key parameters are well matched among the four devices for high-accuracy-and-performance multi-amplifier design opportunities.

Quad devices save board space and reduce inventory and assembly operations, especially important in closely clustered op-amp designs, e.g., active filters, cascaded amplifiers, multiple-channel systems, and instrumentation amplifiers. In addition, a well-designed quad has inherent matching of ac and dc parameters affected by temperature and operating conditions; the ability to track is useful for drift cancellation.

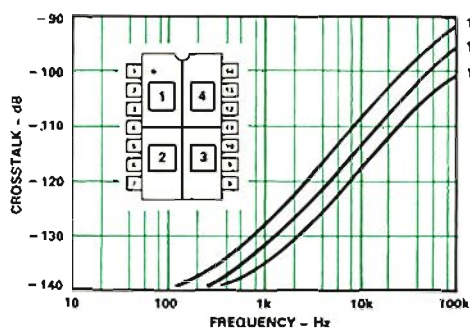
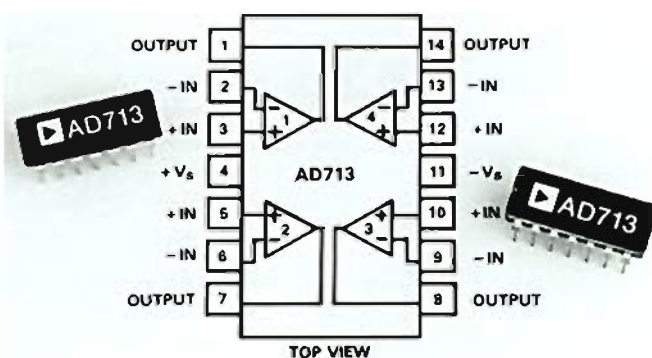


Figure 1. Crosstalk versus frequency.

The AD713 is internally compensated for stable unity-gain operation, with single-pole response and 1- μ s settling time to 0.01%. Typical slew rate is 20 V/ μ s, tested for 16 V/ μ s (min). Typical small-signal gain-bandwidth is 4 MHz, with full-power response (20 V p-p output) to 200 kHz. Total harmonic distortion of 0.0003% meets the needs of demanding audio applications.

DC performance is commensurate with 12- and 14-bit applications. The highest-performance grade's initial input offset voltage is <0.5 mV with drift less than 20 μ V/ $^{\circ}$ C. Open-loop gain is >200 V/mV. From 0.1 to 10 Hz, noise is only 2 μ V p-p.

Crosstalk: A quad op amp's potential weakness, crosstalk from one internal device to another, is minimized by careful electrical

and thermal IC design. Figure 1 shows output crosstalk vs. frequency for device 1, driven by a 2-V p-p sinewave, with the inputs of the other three amplifiers grounded: <-90 dB at 100 kHz for the closest device, 4; less for 2 and 3.

Matching Characteristics indicate how closely the parameters of the four devices track one another initially and with temperature. Input offset voltage, drift, and bias current are matched to within 0.8 mV, 25 μ V/ $^{\circ}$ C, and 25 pA, respectively, for the AD713.

Closely matched devices are useful in active filters. In Figure 2, a single IC is used in a circuit to simulate two coupled inductors (gyrator) in a 1/3-octave bandpass filter, such as is used in audio spectrum analyzers. The filter can handle a 7.07-V rms signal with THD <0.002% from 20 Hz to 20 kHz. Performance meets ANSI Class II specs for rolloff smoothness, shape factor, and passband flatness. Figure 3 shows its amplitude response.

The AD713 has two performance levels for three temperature ranges in plastic DIP or hermetic Cerdip packages. MIL-temp versions are available with processing to MIL-STD-883B. Prices for the 0 $^{\circ}$ -to-70 $^{\circ}$ C K/J-grades in plastic are \$5.95/\$3.50 (100s).

The AD713 was designed by Scott Wurcer, of Analog Devices Semiconductor, Wilmington, MA.

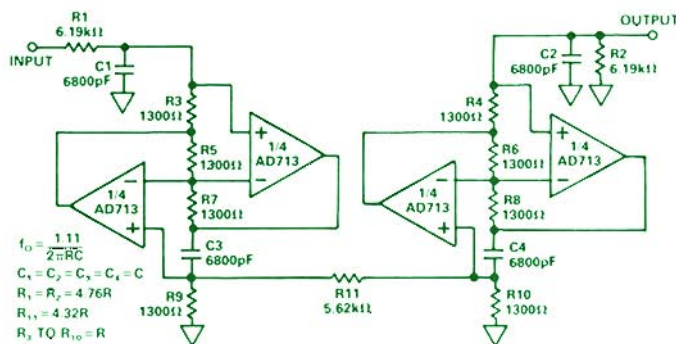


Figure 2. A 1/3-octave active filter.

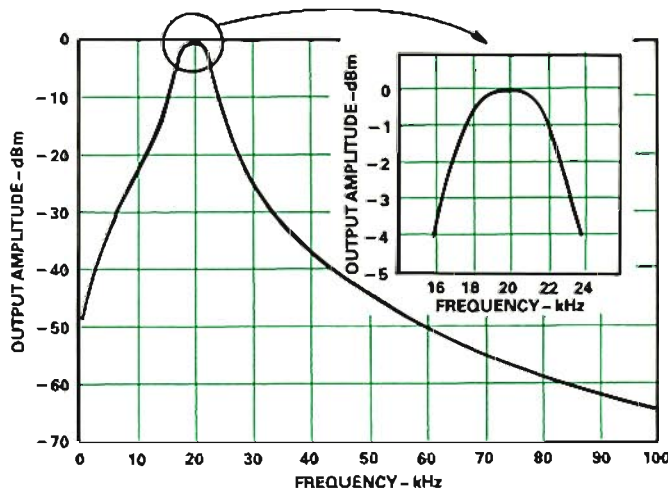


Figure 3. 1/3-octave active filter amplitude vs. frequency.

*Use the reply card for technical data.

12-BIT MONOLITHIC ADC SAMPLES AT UP TO 100KHz

CMOS AD7878 Has 8-Word FIFO to Unburden Processor
72-dB min Signal-to-Noise at 10 kHz, On-Chip Reference

The AD7878* (Figure 1), a complete 12-bit sampling a/d converter for interfacing with digital signal processors, includes on a single CMOS chip (95.5 mW max dissipation):

- track/hold with 2- μ s max acquisition time
- 7- μ s analog-to-digital converter
- 3-volt buried-Zener reference
- 8-word FIFO and interface logic.

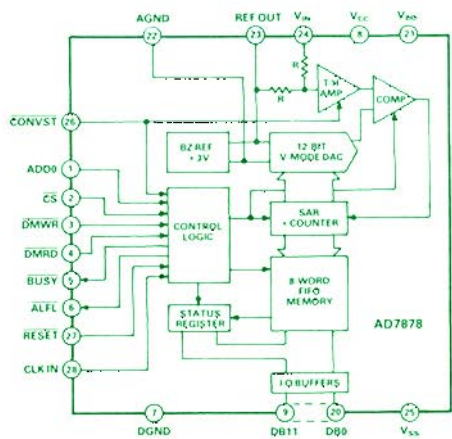


Figure 1. Block diagram of the AD7878.

Typical applications include speech recognition, speech encryption/decryption, modems, radar and sonar signal-processing, and vibration-signature analysis.

The AD7878 is designed to interface easily with high-speed digital signal processors, such as the ADSP-2100 (Figure 2), TMS32010, and TMS32020. The on-board FIFO (first-in, first-out) latch allows for up to eight data samples to be acquired and stored before the processor is required to read, greatly reducing the software overhead associated with servicing processor interrupts.

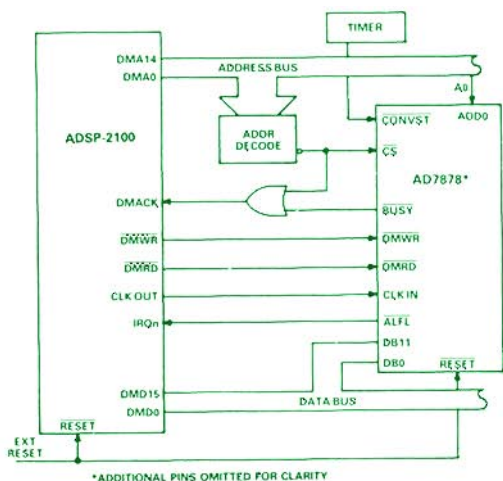
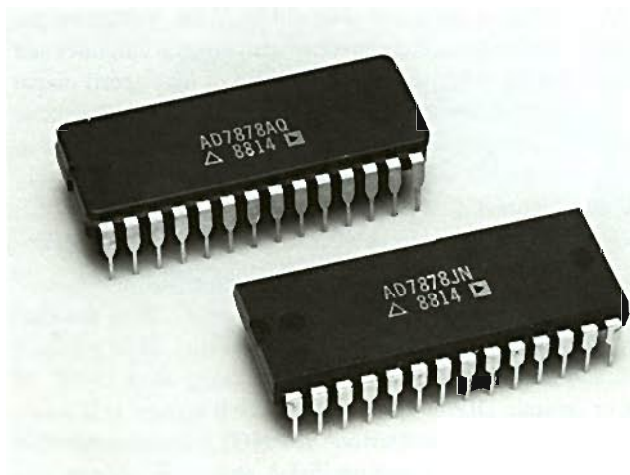


Figure 2. Interfacing AD7878 to the ADSP-2100.


*Use the reply card for technical data.



The eight words that were stored can then be read out of the FIFO at maximum processor speed. An on-chip status-control register allows the user to program the effective length of the FIFO and contains the "FIFO out of range," "FIFO empty," and FIFO word-count information.

The analog input of the AD7878 has a bipolar range of ± 3 volts and the device can convert full-power signals of up to 50 kHz. It is fully specified and tested for ac parameters, including signal to noise (SNR), harmonic distortion, and intermodulation distortion. At an input frequency of 10 kHz, sampled at 100 kHz, the SNR is 72 dB minimum at +25°C—and 71 dB over temperature—(for K, L, B grades, 70 dB minimum for all other grades); all forms of distortion are less than -80 dB max. Figure 3 is a typical plot of the effective number of bits (ENOB) as a function of frequency with 100-kHz sampling.

The AD7878 is fabricated in linear-compatible CMOS (LC²MOS), an advanced mixed-technology process that combines precision bipolar circuits with low-power CMOS logic. Available packages are 28-pin plastic or ceramic (Cerdip) DIPs, and plastic or ceramic chip carriers. Available grades for the three popular temperature ranges are J/K/L (0 to +70°C), A/B (-25 to +85°C, and S (-55 to +125°C). Minimum data-access time over the specified temperature range is 41 ns for the L grade, 57 ns for all others. Prices start at \$28 (JN grade in 100s).

The AD7878 was designed by Dick Meaney at Analog Devices BV, Limerick, Ireland. 

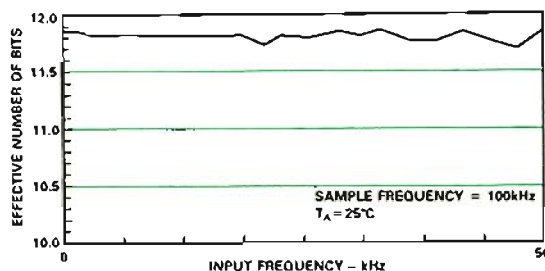


Figure 3. Effective number of bits vs. frequency.

FIRST COMPLETE LOW-COST 12-BIT IC MDAC HAS ON-CHIP AMPLIFIER

AD7845: All Grades Guaranteed Monotonic over Temperature

Ideal for PGAs, D/I Converters, and Programmable Power Supplies

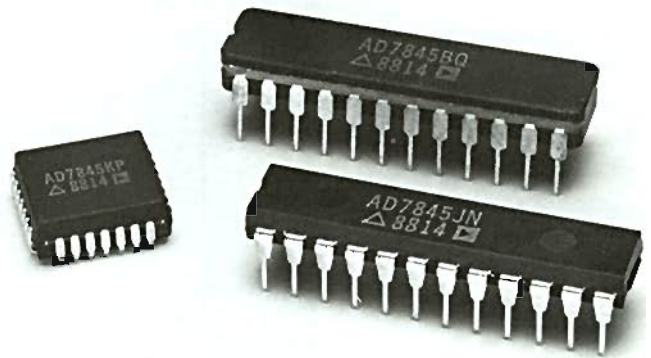
The AD7845* is a complete monolithic 12-bit voltage-output multiplying digital-to-analog converter with on-chip amplifier and extra gain-scaling resistors. Its combination of high-speed digital logic and precision linear circuitry in a 0.3" skinny DIP reduces system chip count and displaces half the space required for traditional 24-pin double-width DIP packages. Interfacing easily to popular 16-bit microprocessors, the AD7845 is the most cost-effective selection for use in automatic test equipment, programmable power supplies, and digital attenuator circuitry.

Its single chip includes (Figure 1) a basic 12-bit CMOS d/a converter, plus μP -compatible latches, control logic, an output amplifier, and gain-setting resistors, all packaged in a choice of plastic or ceramic DIP or 28-pin leadless chip carrier. It is fabricated using the Analog Devices LC²MOS (linear-compatible CMOS) process, which allows precision linear components and digital circuitry to be implemented on the same chip.

The AD7845 provides a compact low-cost solution to requirements for microprocessor-compatible multiplying d/a converters. It can be used to upgrade circuit designs that employ DACs and external op amps for such applications as programmable-gain op amps and attenuators, digital-to-current converters, and programmable power supplies. When driven from a "push-pull" analog source, it will serve as a 4-quadrant multiplier (\pm digital gain \times \pm analog signal, with appropriate output polarity).

The output amplifier can furnish a ± 10 -volt output into a 2-k Ω load. It is internally compensated, and its input offset voltage is low due to laser trimming at the wafer stage of production. For normal operation, R_{FB} is tied to V_{OUT} ; but the user can alternatively choose R_A , R_B , or R_C to scale the output range.

Guaranteed monotonic over the full operating temperature range, the AD7845 allows a maximum of ± 1 -LSB differential nonlinearity. Devices are available in two performance grades for each of three operating temperature ranges: J/K (0° to 70°C), A/B (-25° to +85°C), and S/T (-55° to +125°C). For the AD7845K, relative-accuracy error is $\pm 3/4$ LSB max over temperature; maximum zero-code offset error is ± 1 mV at 25°C, ± 3 mV over temperature (5 $\mu V/^\circ C$ typical tempco). Besides plastic (N) and hermetic ceramic (Q) skinny-DIP packages, PLCCs and LCCCs will soon be



available, as will MIL-STD-883B processing. Prices (100s) begin at \$7.40/\$9.95 (JN/KN).

Figure 2 shows how simple the basic analog connections are for a digitally controlled 4-to-20-mA current source. In this circuit, feedback around the output amplifier causes V_{OUT} to be whatever voltage is required to drive the FET so as to provide the current value through R_L that will maintain the node at programmed voltage, V_X . An additive current, $2.5 V/R_A$, is summed with the current developed by the 2.5-V reference and DAC circuitry; the sum is converted back to voltage by R_{FB} . With D the value of the digital code, from 0 to $(1 - 1 \text{ LSB} \approx) 1$,

$$V_X = -2.5 D - 2.5/4$$

$$I_L = -V_X/R_L - V_X/R_{FB} = -V_X/R_L (1 + R_L/R_{FB}) \\ = [2.5 D/R_L + 2.5/(4 R_L)](1 + R_L/R_{FB})$$

For $R_L = 158 \Omega$ (a standard precision value), when $D = 0$ (all 0's), $I_L = 4.007$ mA; when $D \approx 1$, $I_L = 4.007$ mA + 16.03 mA = 20.04 mA.

The AD7845 was designed by Peter Real, Colin Franklin, John Morrissey, and Analog Devices Fellow Paul Brokaw at Analog Devices BV, Limerick, Ireland.

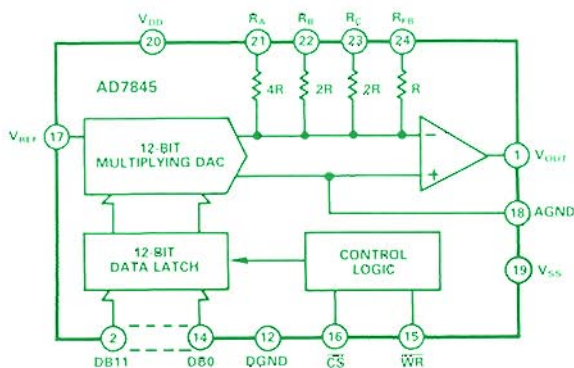


Figure 1. Block diagram of the AD7845.

*Use the reply card for technical data.

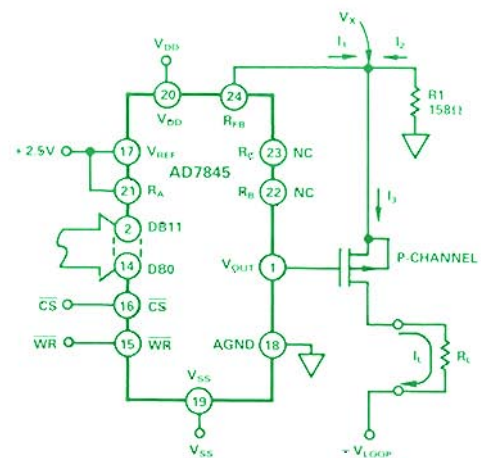


Figure 2. 4-20-mA current-loop application.

12-BIT 10-MSPS SAMPLING ADC IN A DIP

AD9005 is Self-Contained, Including T/H, Timing, Reference, Has Low Distortion, Nonlinearity, and Offset Errors; Low Power

The AD9005* is a complete TTL-compatible 12-bit sampling a/d converter in a 46-pin hermetic metal DIP. It contains a track-and-hold amplifier, voltage reference, and timing circuitry (Figure 1). Using a subranging converter architecture for high speed and resolution, it samples at rates up to 10 megasamples per second (MSPS). Dynamic performance includes SNR of 64 dB and harmonic distortion of -72 dBc, with a 4.3-MHz analog input.

The AD9005 is useful for converting analog signals to digital in any application requiring the combination of high speed and high resolution, especially where space and power are limited. Radar, digital oscilloscopes, analyzers, and communication systems are possibilities. Low gain- and offset errors, wide bandwidth, and low harmonics add to its appeal for most applications. For radar, performance is enhanced by low aperture jitter (20 ps rms max), good transient response (120 ns max to recover to within 1 LSB), and fast overvoltage recovery (250 ns). Low power and small size make it attractive for airborne applications.

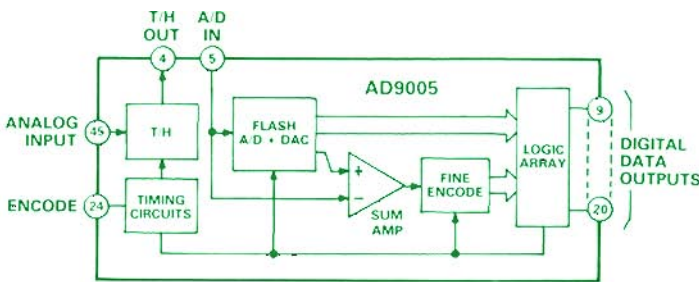
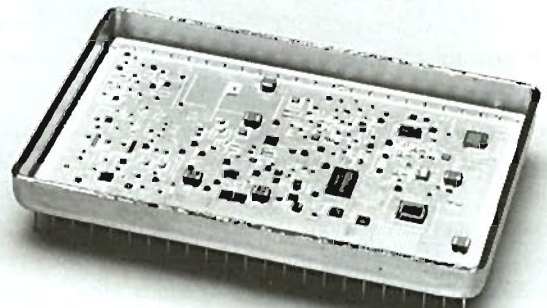



Figure 1. Block diagram of the AD9005.

The AD9005 accepts an analog input range of ± 1.024 V peak-to-peak (250 μ V per LSB), with a large-signal input bandwidth of 38 MHz. Nominal input resistance and capacitance are 1 k Ω and 5 pF. Other specifications include no-missing-codes over the specified operating temperature range, two-tone intermodulation distortion of -65 dBc for (2.2 MHz + 2.3 MHz) signals. Power

requirements are ± 15 volts, +5 V, and -5.2 V. The AD9005 dissipates 3.4 W typical, 4.2 W max; it is the coolest in its class in today's marketplace.

It is available for two operating temperature ranges: AD9005KM for 0° to $+70^\circ$ C and AD9005TM for -55° to $+125^\circ$ C. Unit prices are \$1,200 and \$2,100, dropping to \$800 and \$1,400 in 100s.

Evaluation: As we have indicated on many occasions, (and noted in an earlier article in this issue) high-performance products require considerable care in circuit wiring in order to avoid substantial degradation of performance. For the convenience of interested users who lack the time or resources to design and build an evaluation environment, Analog Devices can make available an evaluation board constructed in accordance with the principles that we advocate; it buffers the analog input, contains a sampling clock, a set of latches, and a voltage-output d/a converter for reconstruction. For information on the availability of such cards, consult the sales force.

The AD9005 was designed by David Duff at the Analog Devices Computer Labs Division, in Greensboro, North Carolina. 

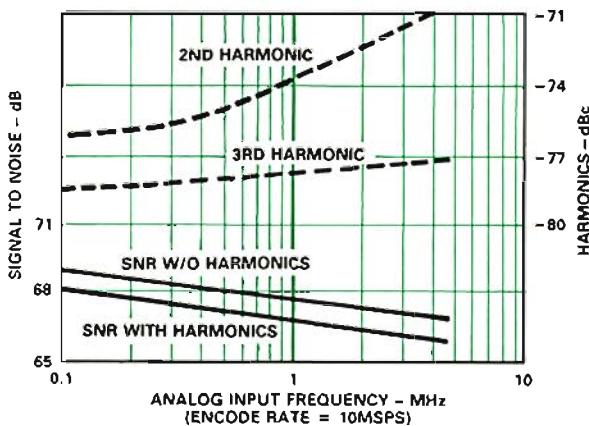


Figure 2. Dynamic performance—SNR and harmonics.

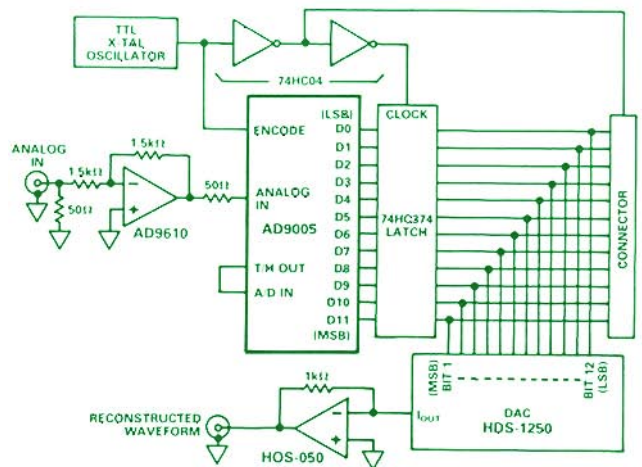


Figure 3. Evaluation circuit.

*For technical data, use the reply card.

MONOLITHIC SERIAL 12-BIT ADC CONVERTS IN 10 MICROSECONDS

AD7772 Is Complete with On-Board Reference, Ranging Resistors Serial Converters Save Space, Have Less Noise, Are Easy to Isolate

The AD7772*, a monolithic LC²MOS serial-output 12-bit, 10- μ s analog-to-digital converter with an on-chip reference, connects directly to a microprocessor's serial bus. The data is strobed, using a serial clock output, as each decision is made.

Since the serial output requires a lot fewer interconnections than a parallel output, it saves space, is easier to connect via electrical isolation (e.g., with opto-isolators) if required, and is well-suited for remote data transmission. In addition, conversion errors due to bus noise are minimized, since a *serial* ADC has only two lines connected to the processor's serial port—plus some control lines (electrical activity on a processor's *parallel* data bus can cause difficulty if (as sometimes happens) coupled back into a converter via its 12 parallel output lines; in such cases, processor activity must be suspended during conversion for full resolution).

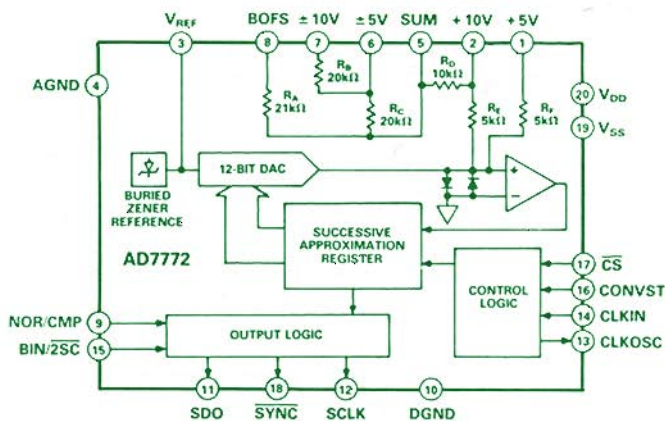
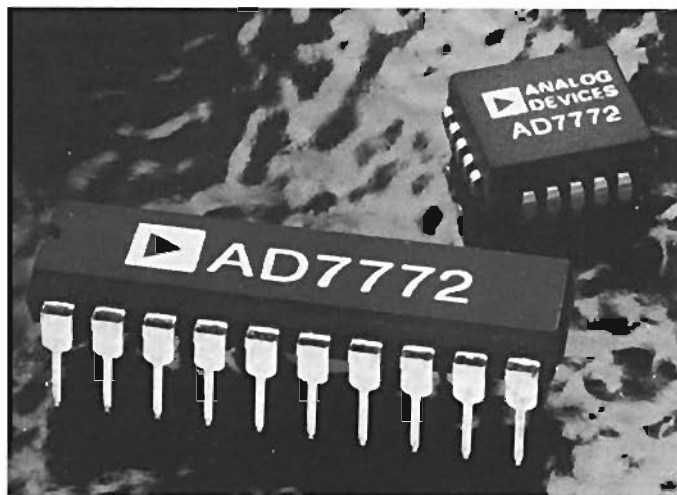


Figure 1. Block diagram.

Figure 1 shows the AD7772's successive-approximations architecture and buried Zener reference. Instead of storing the results of the conversion in a parallel data latch and outputting it through 12 3-state buffers onto a data bus, each comparator bit decision, as it occurs, is latched and outputted through the serial data output (SDO). A serial clock (SCLK) strobes the data, each bit becoming valid on the falling edge of the relevant serial-clock pulse. In order for the user to know which 12 serial clock pulses are associated with valid data, the serial word is *framed* by a low-going $\overline{\text{SYNC}}$ pulse.

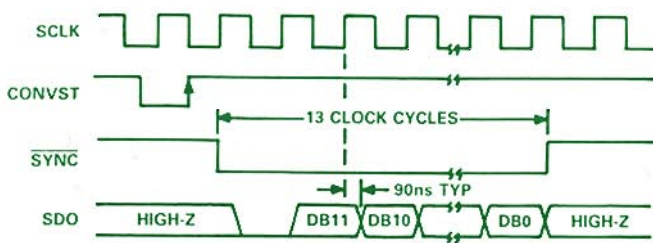


Figure 2. Operating waveforms with an external clock source for CLKIN. CONVST is the conversion Start pulse.

*Use the reply card for technical data.

Figure 2 shows the relationship between the controls, clock, and data. Two control pins allow the data format to suit the analog input range and the processor. For positive analog inputs, binary coding is normally used. With negative inputs, the preferred code is usually 2's complement; the BIN/2^{SC} pin permits a choice. The NOR/CMP pin determines whether the output code is true (straight binary or twos complement) or complementary.

The on-chip scaling resistors permit a variety of analog input ranges: 0 to +5 V, 0 to +10 V, ± 5 V and ± 10 V. Linearity is excellent: maximum differential nonlinearity is ± 1 LSB, with no-missing-codes guaranteed over temperature; integral linearity (L version) is $\pm 1/2$ LSB max over temperature). The AD7772 has two performance grades apiece for two temperature ranges, 0 to +70°C (K, L) and -25 to +85°C (B, C), and is housed in 20-pin skinny DIP and 20-pin PLCC. Prices start at \$35 (100s).

In Figure 3, the AD7772 is interfaced to the ADSP-2101* digital signal processor (available in spring of 1989). The AD7772's $\overline{\text{CS}}$ is tied permanently low. In a sampling system, the Sample Timer controls the start of conversion; when not sampling, the processor's FO pin can control CONVST. When conversion begins, $\overline{\text{SYNC}}$ goes low, framing the serial pulse; the processor accepts data at DR on each negative-going SCLK edge. The ADSP-2101 accepts 12-bit words without requiring shifting and can be auto-buffered for low-overhead data buffering.

The AD7772 was designed by Tony Dunne at Analog Devices BV, Limerick, Ireland.

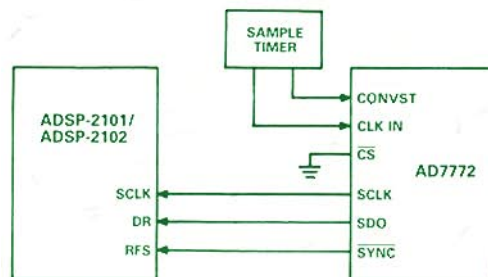


Figure 3. Interfacing to ADSP-2101 digital signal processor.

VOLTAGE-TO-CURRENT ISOLATOR ALSO SUPPLIES LOOP POWER

1B22 Provides 1,500-V rms Isolation in Small Package at Low Cost

Output is 4-to-20 mA or 0-to-20 mA with 28-VDC Compliance

The 1B22* voltage-to-current converter provides current output for process-control applications that require electrical isolation between a signal source (e.g., a programmable controller) and a load (e.g., a valve or actuator). It is functionally similar to the 1B21 voltage-to-current converter (*Analog Dialogue* 22-1), with one major difference: the 1B22 supplies the power for the output loop via its own isolated, internal dc/dc converter.

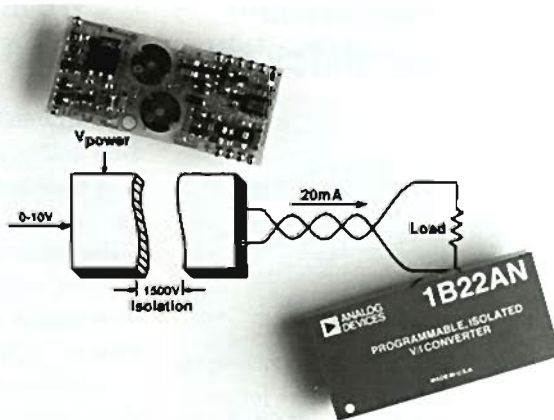
The 1B22 receives a high-level voltage (0 to +5 V or 0 to +10 V) and provides an isolated 4-to-20 mA or 0-to-20 mA output; both input and output ranges are pin-programmable. For additional flexibility, the input range can be set to values between 0 to +1 V and 0 to +10 V with an external resistor. The 1B22 is powered by ± 15 V supplies and a +14- to +30-V supply (to generate power for the isolated loop). No loop power supply is needed.

Magnetic coupling provides $\pm 1,500$ -V rms isolation with low nonlinearity, typically 0.02% of span (0.05% maximum). Using surface-mount technology, the module is only 1.0" \times 2.1" \times 0.35", ideal for multiple-channel systems, where high output-channel density is needed or circuit boards are close together.

The major functional sections of the 1B22 (Figure 1) are the programmable-input amplifier, modulator/demodulator, isolated loop supply, and the output current source. Input range is selected via a resistor network on the inverting input amplifier. The scaled signal modulates a carrier to develop a square wave with peak-to-peak amplitude proportional to the input voltage.

This signal is applied to the signal isolation transformer, specified to provide isolation to 1,500 V rms ($\pm 2,000$ V dc, continuous). The transformer output signal, demodulated and filtered by a single-pole filter, is the control signal for the voltage-to-current converter stage. Demodulator phase information is derived from the output of the internal dc-to-dc converter's power transformer.

Figure 2 shows a typical connection scheme. The dc-dc converter provides power for the output circuitry and isolated power for the loop. Loop compliance is proportional to the voltage supplied for loop power; with 28 V dc applied, the 1B22 can drive 1,000 Ω . Isolation eliminates ground loops; the level provided meets IEEE Standard 472 (Surge Withstand Capability) for Transient Voltage Protection ($\pm 2,500$ V peak CMV). Outputs are protected from accidental shorts to line voltage up to 240 V rms.



External Loop versus Internal Loop Power Supplies Whether to use an external loop power supply with a 1B21 converter or the internally supplied loop power of the 1B22 is determined by required performance, cost, and the nature of the application. For multiple outputs, each 1B22 provides essentially the same functionality as a 1B21 with an isolated supply. A saving can be realized with multiple 1B21s, using a single common external supply to maintain input-to-output isolation; but channel-to-channel output isolation is lost.

When isolation serves mainly to protect the signal source or instrumentation from loop CMV, a common loop supply is acceptable. But to protect loops and loads from one another's high CMVs, channel-to-channel isolation must be maintained. With 1B21s, a separate supply for each loop is costly and space-consuming; instead, using 1B22s and a single power source, loop power can be provided to multiple loops with channel-to-channel isolation, since loop power transits an isolation barrier within each device.

When multiple 1B22s are used in close proximity, their oscillators can be synchronized—via a SYNC pin driven at 40 kHz—to prevent beat-frequency-related errors. Specified for performance from -25° to $+85^{\circ}$ C, the 1B22 can operate at temperatures down to -40° C. It is priced at \$52 (100s).

The 1B22 was designed by Alan Jeffery, at the Analog Devices Industrial Products Division, Norwood, MA.

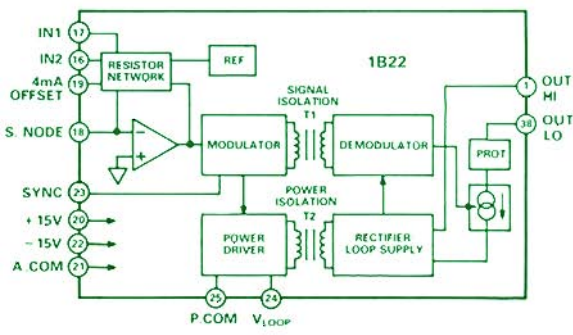


Figure 1. Block diagram.

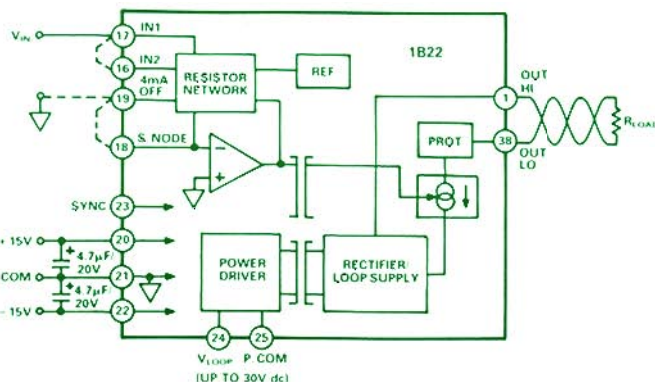
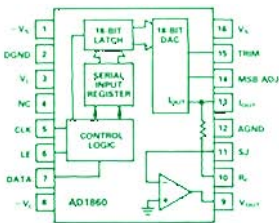


Figure 2. Basic Interconnections.

*Use the reply card for technical data.

18-BIT AUDIO DAC

AD1860: Low Distortion PCM For CDs and DATs



The AD1860* is a proprietary monolithic 18-bit digital-to-analog converter for audio applications. It is designed specifically for compact-disc players, digital audio tape (DAT) players and recorders, synthesizers, digital audio amplifiers, and keyboards.

Fabricated on a single BiMOS chip and housed in a 16-pin DIP, it includes a voltage reference, voltage-output amplifier, switch circuitry, laser-trimmed thin-film resistors, and logic interface—eliminating the need for as many as 24 external components.

The AD1860 provides audio designers with the simplest available upgrade path from 16- to 18-bit resolution. A serial-input device, it is pin-for-pin compatible with popular 16-bit audio DACs, such as the AD1856* and PCM56. The extra resolution permits total-harmonic-distortion-plus-noise (THD+N) to be improved with no major circuit changes.

Capable of 2×, 4×, and 8× oversampling, it accepts serial data directly from second-generation digital filter chips at rates up to 12.7 MHz. Output is ±3-V (peak) or ±1 mA (peak), with 108 dB of dynamic range.

Operating from ±5-V to ±12-V supplies, the AD1860 dissipates as little as 105 mW. Typical signal-to-noise (SNR) is 107 dB. The internal amplifier, with short-to-ground protection, has a 9 V/μs slew rate and 1.5 μs settling time to 0.006% of full-scale range for a 6-V input step. Typical differential-linearity error is ±0.001% FSR.

A companion 16-bit DAC, the AD1856, is also available. Specified for operation from -25 to +70°C, and 100% tested and graded for (THD+N), both are available in three grades. Prices begin at \$10.70/\$19.50 (AD1856/60) in 1000's.

*Use the reply card for technical data.

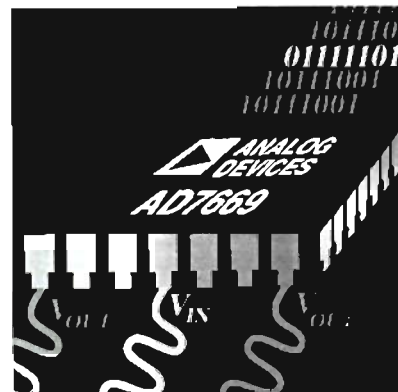
8-BIT ANALOG I/O PORT: ADC, T/H, AND 2 DACS

**AD7669 Is Complete on a Single Chip
ADC Converts in 2 μs; DACs Settle in 2 μs**

The AD7669* is a complete monolithic 8-bit analog I/O port; it has an 8-bit ADC with track/hold, two 8-bit DACs with output amplifiers, a bandgap reference, and digital interface logic. It saves space and is a low-cost solution in systems that need to both digitize and synthesize analog signals, with or without intermediate digital processing; examples include servo loops, automatic calibration systems, and bar-code readers.

Except for the additional *d/a* converter, its architecture is like that of the AD7569, recently featured in these pages (21-2, 1987, pp. 3-5); both units are specified on a common data sheet.* Although generally useful in systems where more than one output is needed, the additional DAC comes in especially handy in vector operations, where analog X and Y outputs are required.

Bus timing of the AD7669 is compatible



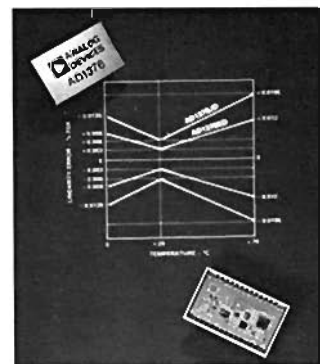
with all modern μPs, with 60-ns bus-access and -relinquish times and <80-ns Write pulsewidth. The AD7669 is fully specified in terms of dc, system, and ac dynamic specifications (sinewaves of 100 kHz for the ADC and 20 kHz for the DAC). At present, the AD7669J is available for 0 to 70°C operation in plastic DIP or PLCC packages. Prices (100s) start at \$9.50.

16-BIT, 16μs PARALLEL/SERIAL ADC AD1376 Is Complete in DIP with Industry-Standard Pinout Maximum Linearity Error Is Less than ±0.003% (KD Grade)

The AD1376* is a 16-bit, 16-μs analog-to-digital converter in a 32-pin ceramic DIP. It is similar to the AD376 (*Analog Dialogue* 19-1, 1985), but with lower cost; and it is form, fit, and function compatible with the ADC76; but its no-missing-codes specs apply over the full 0 to 70°C temperature range.

A complete device, including reference and clock, the AD1376 is designed for use in high-speed, high-resolution-and-high-accuracy data-acquisition systems. Applications include ATE and analytical and medical instrumentation.

The KD grade has a maximum linearity error of ±0.003% of full-scale range and guarantees no missing codes over temperature for 14-bit resolution. Conversion can be short-cycled in a tradeoff of bits for conversion speed; for example, while conversion to 16 bits takes 15.5 μs (17 μs max),



conversion to 14 bits is complete in 13.5 μs typical, 15 μs max.

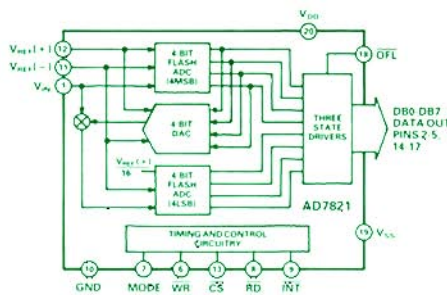
On-board scaling resistors allow a choice between 0 to +10 V, 0 to +20 V, ±2.5 V, ±5 V, and ±10 V. Output is complementary binary for unipolar and complementary offset binary for bipolar signals. Two performance grades are available (JD/KD). Prices (100s) are \$103/\$124.

8-BIT 600-ns IC SAMPLING A/D CONVERTER

AD7821 Is an Improved 0820: 2 × Speed, 14 × Signal BW Accommodates Unipolar & Bipolar Signals, No Extra Cost

The AD7821* is a high-speed alternative to the AD7820 and the industry-standard 0820 type of 8-bit a/d converter. The CMOS AD7821 delivers conversions in half the time—600 ns vs. 1.36 μs—and with more than 14 times the signal bandwidth—100 kHz vs. 7 kHz—of other 0820 designs. In addition, the AD7821 accommodates both unipolar and bipolar input ranges. The performance increases are available at no additional cost. Prices for the AD7821 start at \$9.95 in 100s (AD7821KN).

The AD7821 uses two 4-bit flash ADCs in a subranging architecture; since the technique employs only 31 comparators, instead of the 255 required for a normal 8-bit flash converter, the device can be manufactured at lower cost. The design includes an inherent track/hold function, eliminating the need for a separate T/H amplifier. For bipolar ranges (unique with the AD7521), $-V_{SS}$ is connected to pin 19, nor-



mally unused in the 7820 and 0820 devices; for unipolar ranges, that pin is simply grounded for total compatibility with the other types.

Minimum SNR is 45 dB, maximum distortion (harmonic or IM) is -50 dB, and maximum slew rate is 1.6 V/μs. Power required is +5 V (unipolar) or ±5 V (bipolar). The three common temperature ranges are available (K, B, T) and 20-pin packaging options include plastic and ceramic DIPs (N, Q) and LCCs (P, E). ▶

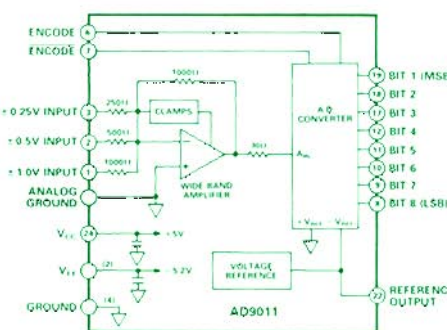
8-BIT 100-MSPS COMPLETE BUFFERED ADC

AD9011: Flash Converter, Buffer Op Amp, And Reference Hybrid in 24-Pin-DIP Saves Board Space And Design Time

The AD9011* combines the AD9002* 8-bit flash converter (*Analog Dialogue* 21-1), a modified AD9611* op amp (22-1) and a voltage reference into a 24-pin hybrid. This saves board space and eliminates optimizing the performance of an op amp to the flash converter. Users gain time to complete a project and engineering design resources are enhanced.

All digital inputs and outputs are ECL-compatible. No-missing-codes is guaranteed over the full temperature range. Typical application areas include military radar, EWS, digital oscilloscopes, and data recorders.

A fast-recovery circuit protects the flash's input. Typical recovery time to ±1 LSB from a 1.5×FSR overvoltage is 20 ns. Bipolar analog inputs and pin-programmable AIN (2 V, 1 V, 0.5 V peak-to-peak) add



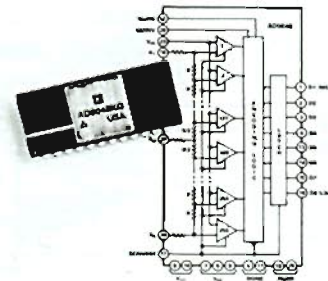
flexibility. The internal reference provides up to 12 mA at -2 V for external needs.

Packaged in a 24-pin metal DIP, the AD9011 operates from +5.0 and -5.2-volt supplies and is available specified in two grades each for the 0 to +70°C (JM/KM) and -55 to +125°C (SMB/TMB) temperature ranges. KM & TMB grades have maximum linearity error of 0.5 LSB (0.75 LSB for JM & SMB). Prices start at \$180 in 100s. ▶

*Use the reply card for technical data.

8-BIT VIDEO ADC

Improvement on TDC1048 Higher Speed, Lower Power



The AD9048* 8-bit monolithic flash ADC, an alternate for the TDC-1048, has a greater conversion rate and input bandwidth, with lower input capacitance (16 pF). Well-suited for real-time conversion of video signals, the AD9048 combines a 10-MHz input bandwidth and a minimum 35 MSPS (million-samples-per-second) conversion rate without degradation to the signal-to-noise ratio or dynamic performance. Lower input capacitance reduces analog phase shifts and drive requirements.

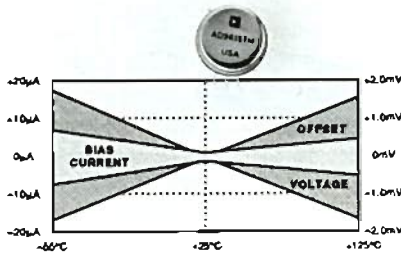
It is an especially attractive and cost-effective pin-compatible second-source device for military instrumentation, digital radio, electro-optic, and medical equipment. On-board strobed latching comparators, encoding logic, and output buffer registers, operating at 35 MHz, reduce the need for sample/hold circuits in most applications. No-missing-codes is guaranteed over temperature. Control inputs and 2's-complement outputs are TTL-compatible.

The lowest-cost grades (J/S) have 0.75-LSB max nonlinearity (differential and integral), 1 LSB over temperature. Signal-to-noise (SNR) is 44 dB and 40.5 dB for 1.248 and 9.35 MHz inputs; in-band harmonics are -48 dBc for inputs from dc to 9.35 MHz. Settling time to 8-bit accuracy (full-scale step) is 20 ns max. Typical recovery time (-3-V input overvoltage) is 8 ns. Maximum aperture delay and jitter are 5 ns and 50 ps.

Power required is at +5 V and -5.2 V, with 550-mW dissipation. Temperature ranges are 0 to +70°C (J/K) and -55 to +125°C (S/T). The K/T grades have 0.5-LSB nonlinearity. Packages include 28-pin plastic (N) or ceramic (Q) DIPs, PLCCs (P), and LCCs (E). Prices (100s) start at \$20. ▶

200-MHz OP AMP

8 ns to 1%, 13 ns to 0.1%
— 88 dBc 2nd HD @ 1 MHz




The AD9615* is a new hybrid transimpedance op amp (see page 13) that combines high speed and dc precision to offer exceptional dynamic performance. It settles to within 1% in 8 ns and to 0.1% in 13 ns, with rise- and fall times of 2.6 nanoseconds. Its dc specs are attractive, too: $\pm 250 \mu\text{V}$ typical input offset voltage with $3 \mu\text{V}/^\circ\text{C}$ drift, $\pm 0.5 \mu\text{A}$ bias current, and $\pm 20 \text{ nA}/^\circ\text{C}$ input bias drift for both inputs.

High-speed signal-processing calls for low noise and distortion. With a 20-MHz input tone, 2nd-harmonic distortion is typically -62 dBc, dropping to -88 dBc for 1 MHz. The proprietary output stage contributes to the low distortion and reduces thermal problems common to wideband amplifiers. With bandwidth limiting, it can be used in 14-bit systems.

Typical applications include input buffers for ADCs and output amplifiers for DACs; photodiode preamps; and IF signal processors for radar, communications, and spectrum analyses of video imaging.

No external compensation circuitry is required. Its design as a transimpedance amplifier with low inverting input impedance (18Ω typical) results in bandwidth that changes little with closed-loop gain. Its current-steering output design keeps its power dissipation constant at 670 mW typical as a function of load.

Packaged in a 12-pin TO-8 metal can, the AD9615 operates from $\pm 5\text{-V}$ supplies. The "TH" version operates in ambient temperatures from -55 to up to 116°C without a heat sink (125°C with airflow). The "BH" version is specified from -25 to $+85^\circ\text{C}$. Pricing begins at \$79 (100's). 

*Use the reply card for technical data.

LADDER-LOGIC HARDWARE & SOFTWARE


Create and Edit Ladder-Logic Programs on an IBM PC
Download Them to the $\mu\text{MAC-6000-L-87}$ Target System

Software for the Analog Devices $\mu\text{MAC}^{\text{®}}$ -6000 (*Analog Dialogue* 20-2) provides ladder-logic programming capability for analog and discrete I/O. PROM-based SFT03* on-board software provides standard ladder-logic functions, extended math capability, and PID control functions.

Traditional ladder logic is combined with the analog-I/O effectiveness of the $\mu\text{MAC-6000}$ for programming ease and maximum capability in a high-channel-count analog I/O system that can measure inputs, perform calculations (enhanced for P-I-D loops by the $\mu\text{MAC-6000}$'s 8087 co-processor), make decisions, and generate control outputs. The software, developed on a PC and downloaded to the $\mu\text{MAC-6000}$ via RS-232, supports 8,000+ elements per file, 40 step-per drum screens, 40 PID loops, rung-by-rung load and test, on-line monitoring of relays and coils, timer and counter functions, and "help" screens.

I/O can be monitored on the screen while the ladder program is executing. The Con-



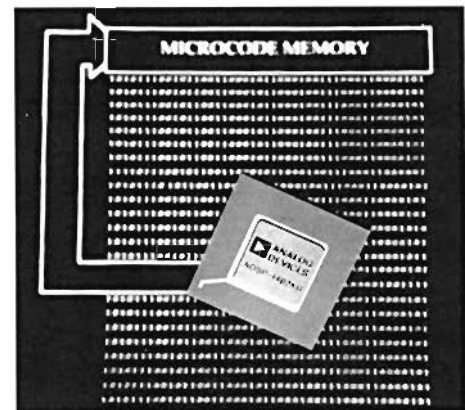
trol Process, Inc., Relay Ladder Logic[®] software is available from ADI with a licensing agreement. Prices are \$995 for the software development package, SFT03, and \$3,725 (plus I/O) for $\mu\text{MAC-6000-L87}$. 

PROGRAM SEQUENCER FOR MICROCODE


ADSP-1402 Supports 20-MIPS Systems
Code-Compatible with First-Generation ADSP-1401

The ADSP-1402* Program Sequencer's proprietary Look-Ahead[™] pipeline and $1\text{-}\mu\text{m}$ CMOS technology support 20 MIPS systems. In addition, system design using the ADSP-1402 microcoded system is simplified by a 64×16 RAM for implementing an on-chip stack, four event counters for looping, provisions for downloading microcode, facilities for processing exceptions from arithmetic units, and flexible interrupt handling for prioritized interrupts.

Fully instruction-compatible with the ADSP-1401 (*Analog Dialogue* 20-1), it supports absolute, relative, and indirect addressing, as well as an extensive set of branch instructions, including subroutine calls and conditional branches on external events; all branch instructions execute in a single cycle. New features of the sequencer include: a HALT pin to implement system



Wait states, an 8-way condition MUX to ease critical flag-timing requirements, and a single external pin to initiate a download to microcode memory.

The ADSP-1402 is packaged in an 84-lead PGA. Prices start at \$47 in 1,000s. 

MULTI TROUBLES

Q: *My multiplexed ADC system is misbehaving . . .*

A: Before you go any further, have you grounded all unused multiplexer channels?

Q: *No. But how did you know?*

A: Because the floating terminal is one of the commonest causes of problems in systems containing CMOS multiplexers. Unused MUX inputs and outputs (whether integrated into a multiplexed ADC or part of a self-contained MUX chip) can pick up signals from stray fields and inject them into the device's substrate, turning on spurious substrate devices. Then, even when the unused channel is turned off, the performance of the *on*-channel may be badly degraded (at the unlikely extreme, the injection may turn on a spurious four-layer device and destroy some chips).

Whenever a MUX is used, all its inputs and outputs must be connected to a potential between its supply rails. The best way to deal with unused channels is to ground them, but they may be connected to a more-convenient potential within the rails. ▶

TROUBLE FROM THE START

Q: *To save power, my ADC is powered up only to make a measurement. The system is very accurate in continuous operation, but unpredictable when power is strobed. Why?*

A: When an ADC's power is switched on only to perform a conversion, it may misbehave for three reasons: slow reference turn-on, random initial logic states, and system latch-up.

For various reasons—thermal stabilization, capacitance charging, slow starting of regenerative current mirrors using PNP transistors in band-gap references—it is not uncommon for some voltage references to have relatively large errors for many milliseconds after power-up. Such errors in an ADC's external or internal reference during conversion lead to inaccurate results.

At turn-on, a typical ADC's logic will be in a random state; for a conversion triggered at that time, the ADC may not be able to perform correctly. With one conversion triggered, the logic should return to its correct pre-conversion state—but cases exist where two conversion cycles are necessary before the ADC is certain to perform a valid conversion. Hence, a good general rule is to perform two "dummy" conversions after powerup before relying on the results. (It is also well to recall that some ADCs react badly to having a conversion triggered before the previous conversion is complete; when this happens, one or two "dummy" conversions may be needed to return the logic to a known state.)

If an ADC's external logic is arranged so that the end of the ADC "Busy" signal starts a delay which ends with the start of the next conversion, it is important to realize that if the converter powers up in the Busy state, the Busy signal may remain latched up until a conversion Start pulse has been received. In this case, such a system cannot self-start. If the Busy signal is always present on power-up the problem is almost certain to be recognized—and addressed—during the

design of the system; but if the Busy signal is only occasionally present on power-up the system may latch unpredictably. As a rule, control signals to an ADC during start-up should not depend on the logical state of Busy. ▶

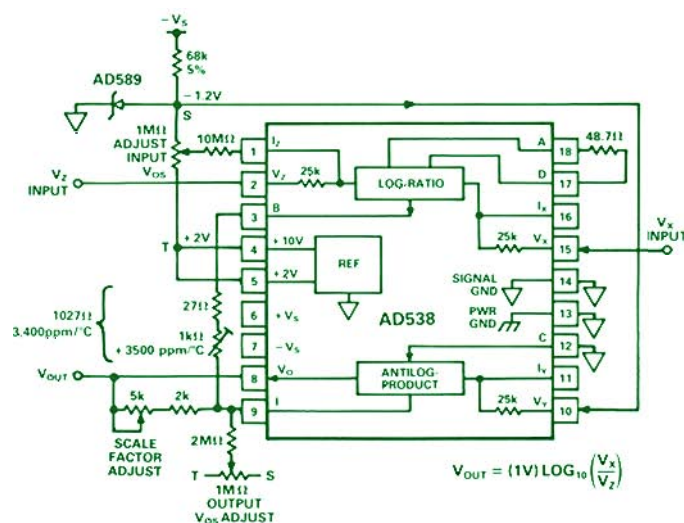
ABOUT LOG COMPENSATION RESISTORS

Q: *Designs of logarithmic circuits*, including those using the AD538 $Y[Z/X]^m$ unit: (for example, Figure 6 from the AD538 Multi-function Unit data sheet†) call for "kT/q compensation resistors". What are they and where do I get them?*

A: The V_{BE} difference across two opposed silicon junctions, one carrying a current, I , and the other a current, I_{REF} , is $(kT/q) \ln(I/I_{REF})$. Here, k/q is the ratio of Boltzmann's constant to the charge on an electron (about 1/11,605 K/V), and T is the absolute temperature in kelvins.

Although employing similar junctions in isothermal pairs eliminates the effects of temperature-sensitivity of reverse saturation current, the kT/q is still temperature-dependent. To eliminate this dependency in the application, the logarithmic voltage must be used in a circuit whose gain is inversely proportional to the absolute temperature of the junctions. Over a reasonable range of temperatures near 20°C, this may be arranged by the use of a gain-setting 1-kΩ resistor having a positive temperature coefficient of approximately 3,400ppm/°C—and keeping it at the same temperature as the junctions.

A 3,500 ppm/°C resistor is available from Tel Laboratories, 154G Harvey Road, Londonderry, New Hampshire 03053 (603)-625-8994, Telex: (710)-220-1844, designated Q-81, and from the Precision Resistor Co. Inc., 10601, 75th. St., Largo, Florida 33543 [(813)-541-5771 Telex: 821788], as the PT146. Analog Devices offices in most European countries are aware of local suppliers of these resistors. ▶



*Much useful information about logarithmic and other analog function circuits can be found in the *Nonlinear Circuits Handbook*, published by Analog Devices (\$5.95), P.O. Box 9902, Norwood MA 02062.

†Use the reply card for technical data on the AD538. See also *Analog Dialogue* 19-1 (1985), pp. 3-6.

Worth Reading

SERIALS*

(To subscribe, write or phone Analog Devices or the nearest sales office.)

Since our last report, there are two new issues of *DSPatch—The Digital Signal-Processing Newsletter* (available free upon request), featuring news of DSP products and applications:

Number Eight, June, 1988 (16 pages) features a preliminary look at the ADSP-2101/2, a complete DSP Microcomputer that combines the complete ADSP-2100 architecture with on-board program and data-memory RAM, two serial ports, and other useful features, including an instruction set that is a fully compatible superset of the ADSP-2100's. There are descriptions of products that use ADI's DSP integrated circuits, for example, Digicom Systems V.32 Modem (ADSP-2100) and Tek Graphics Workstations (ADSP-3210 & ADSP-3221). The rest of the issue includes "Q & A"; "How to Talk Analog," about grounding; notes on products, accessories, cross-software upgrades, seminars, third-party consultants; and available literature.

Number Nine, September, 1988 (16 pages) considers application of the ADSP-2101 to the V.32 Modem. Two products that use the ADSP-2100 are described: Synoptics, Ltd.'s "Synergy" IBM PC AT plug-in image-processing and frame-store subsystem for digitizing, processing, and displaying monochrome TV signals, and Data Beta's DBSVSP-1 scalar and vector processor. Other features include "Q & A"; "How to Talk Analog," about sample/track-holds; notes on interfacing the ADSP-2100A to a host; updates on ADSP-2100 sockets and MIL grades; ADSP-3128A data-sheet; bulletin-board number change [to (617) 461-4258]; 3rd-party consulting; product-line overview; seminars; and available literature.

There are also two new issues of *ANALOG BRIEFINGS—The Newsletter for Military/Avionics Industry*

Volume 4, Number 2 has articles on how Computer Labs' self-audit program maintains DESC certification; the AD9521 log amp for radar and ECM; the impact of changes in MIL-M-38510 and Notice 7 changes in MIL-STD-883; two new standard military drawings (SMDs) for high-precision instrumentation amplifiers in the AD625 and AD524 families, used (for example) for sonar and infrared applications; and shortly available SMDs for the /883 versions of 12-bit (AD394 & AD395) and 14-bit (AD396) quad DACs, processed to meet the requirements of MIL-STD-883C, MIL-STD-1772, and MIL-M-38510.

Volume 4, Number 3 features a description of the self-audit program and MIL-M-38510 qualification of our plant at Analog Devices, BV, in Limerick, Ireland. Also in this issue: Three new /883B speed grades of the ADSP-2100 and the ADSP-2100A; ADI's interdivisional round-robin particle-impact noise-detection test (PIND) correlation; qualification of two voltage references—AD589 to /883B and AD580 to SMD 5962-86861XC. Also included is a 6-page insert with an updated listing of all of ADI's military and SMD parts now available.

APPLICATION NOTES*


"The AD9502 Video-Signal Digitizer and Its Application," by Alan Hansford (12 pages) discusses video signal processing, the AD9502 architecture, RS-170 video formats, aspect ratio and

*Use the reply card to request copies.

pixel counts, standard RS-170-to-memory interface, performance and layout enhancements, gain and offset adjustments, digital output buffering and ECL memories, external clock drives, grounding, power-supply decoupling, layout recommendations, power dissipation and heat sinking, genlock and external pixel clocks, 1/2 frame ping-pong, RGB applications, composite color, and European applications.

"Replacing the Am2910 with the ADSP-1401 Program Sequencer," by Gordon Sterling (4 pages) discusses the ADSP-1401 as a highly versatile replacement for the venerable Am2910. Topics include: instruction set, internal memory, address space, interrupt handling, and an instruction-by-instruction consideration of similarities and differences between the two program sequencers.

ARTICLE REPRINT AVAILABLE*

"DSP Microcomputers Cut Pin Count and Retain Performance," by Greg Koker, *Electronic Products*, May 1, 1988. "The ADSP-2101 and ADSP-2102 do it with Harvard architecture, on-chip memory, and dual serial interfaces." An overview of their architecture and key features, including autobuffered data transfers (for very low-overhead transfers of data to and from the serial ports and on-board memory) and the GOMODE (for continued processing while external busses are granted to another processor). 


MORE AUTHORS (Continued from page 2)

Richard Johnson (page 10) is a Product/Test Development Engineer in the Linear Systems Automation Converter Operating Group at Analog Devices Semiconductor. He holds a BSEE from Boston University and is currently working towards his MSEE at BU. In his spare time, he enjoys swimming, weight training, softball, and ice hockey.



Peter Predella (page 18) is a Technical Publicity Associate at Analog Devices, in Norwood MA. Since joining ADI, in 1979, he has also been a Technician for the Component Test Systems and Memory Devices Divisions. Peter is a graduate of GTE Sylvania Technical School and is currently pursuing a BSET from Northeastern University. His interests include reading, salt-water fishing, and golf.



James Bryant (page 29) is European Applications Manager for ADI, based in Newbury, England. A graduate of the University of Leeds, he earned a B.Sc. in Physics and Philosophy. He has 19 years of applications experience, at both Plessey and ADI. James has numerous publications on a wide range of topics and served as a technical advisor to Parliament on CB radio. His diverse interests include amateur radio (G4CLF), collecting science fiction (>3,000 volumes), hypnotism, and parapsychology. 



An Electric Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

ERRATA . . . In the Data Converter Products Databook, the AD394/5/6 ceramic bathtub package option should be listed as the (wider) bottom-brazed-DH-28A. This information is correctly listed in the 1987 Military Products Databook . . . 1B21 and 1B22 data sheets pin spacing on the outline drawings should be corrected as follows. 1B21: pins 1 & 38 to end and pins 19 & 20 to end: 0.15" (3.81 mm); 1B22: pins 1 & 38 to end: 0.15" (3.81 mm) typ, pins 17 & 22 to end: 0.35" (8.9 mm) typ . . . AD9615 data sheet: The internal resistor (block diagram on page 1) should be 1.5 k Ω .

NEW-PRODUCT CLIPS (Write to ADI or consult the sales force for further information) . . . CMOS switches and multiplexers are available in 16- and 18-pin small-outline packages (SOIC), in addition to 20-pin PLCCs. Some converters can also be made available in SOICs, e.g., the AD7528 & AD7820 . . . Some recent product releases in surface-mount packaging: AD573, AD673, AD557 . . . 2S82, a surface-mount version of the 2S80 Resolver-to-Digital Converter, with additional features: complement output, VCO output, and a good-quality velocity output . . . Low-cost IBM PC/XT/AT-compatible plug-in evaluation board for the AD1170 18-bit programmable integrating ADC (complete with menu-driven evaluation software and a User's Guide). Your PC can function as a 5-digit voltmeter; ask about the AC5004 . . . DSP: A variety of development support hardware and software for the ADSP-2100 and ADSP-2100A is available and more is coming. Get in touch with Sales or the DSP Division in Norwood MA . . . The AD210JN is a 1,500 V rms continuous isolator at lower cost than the AD210AN . . . The AC1367 Voltage Switch Input Module is a non-isolated 5B-Series signal-conditioning module for connecting pre-conditioned signals to the backplane . . . LABTECH NOTEBOOK now supports all RTI-800-series boards for IBM PCs; ask about AC1529 and AC1530 . . . The SNAPSHOT (AC1911) family now supports RTI-850 and RTI-860; included is SNAP-STREAM (AC1911-STREAM), for streaming to disk (concurrent sampling and storage of 20 million data points at 100-kHz rates) . . . μ MAC-6000 Technical Reference Manuals are available for hardware (AC1866H) and software (AC1866SM or SC); get in touch with the factory or the sales force for prices . . . Intellution's THE FIX, a menu-driven software package for monitoring and control of industrial processes using IBM PCs, supports the RTI-800/815 and 820 I/O boards and μ MAC-4000, 5000, and 6000 measurement-and-control front ends. A new revision of "c" (rev. 2.0) is available for μ MAC-6000.

PRODUCT NOTES . . . ADSP-2100 digital signal processor and ADSP-1401 microcode program sequencer are now available in low-cost plastic packaging . . . Cerdip will replace side-brazed packaging for the AD9685 and AD9687 high-speed comparators . . . AD7572C spec change: Integral nonlinearity (T_{min} to T_{max}) is $\pm 3/4$ LSB max. The corrected data-sheet is numbered C961C-9-7/88 (back page along spine). Also, in the Data Conversion Products Databook, page 3-212, the column labeled "L_U" should be "L_C" . . . AD568 spec change: max digital input low current is -100 μ A for J,K grades and -200 μ A for S. A "Rev. B" data sheet, dated 9 88 documents the /883B version . . . AD8C71/72 now draw 0 mA at the +5-volt terminal (i.e., they no longer require a +5-volt supply); AD8C80/85/87: the logic HI current is now 250 μ A max . . . The AD202, AD204, and AD210, and the 5B Series have a wider operating temperature range: -40°C to +85°C (the rated performance range is unchanged) . . . 1B32: signal common, pin 8, must be connected to pin 16, common, for proper operation . . . AD1147: connect a 7.5-M Ω , 1 $\%$, 10 ppm/°C resistor between pins 3 & 5 to be able to use the internal offset-correction DAC for nulling to zero in the unipolar connection . . . AD9500: ECL common can be tied to potentials other than ground, but not $\geq +5$ V. OR output has limited output capacity when 0 is in use. In early units, data levels should not approach or exceed ± 4 V; In future units, this is not a consideration. Always remember that, as a high-speed analog part, it needs attention to circuit details: power-supply bypass and a low-impedance ground plane are musts, and a clean trigger signal (fast edge) ensures a repeatable delay (low jitter) . . . DAS1157/DAS1158/DAS1159 now contains semiconductors that are not hermetically sealed (all performance specifications remain the same, just a change in that Feature on the data sheet) . . . LTS-1990 Diskless Communications Software (enhanced versions of TEST, CREATE, and MERGE) transforms the LTS-2020 benchtop component tester into a stand-alone workstation, allowing a host computer to maintain storage of programs and test data, perform all sorts of off-line tasks and eliminate floppy diskettes.

MILITARY NEWS . . . Note: Standard Military Drawings (SMDs) are available from: The Naval Publications & Forms Center, 5801 Tabor Avenue, Philadelphia PA 19120 . . . For information on any products mentioned below, get in touch with Analog Devices or the nearest sales office . . . The AD588 monolithic ultra-stable voltage reference now has 5 grades available over the military temperature range, including three /883B versions . . . There are now three /883B versions of the ADSP-2100 and ADSP-2100A digital signal processors . . . Switches: Two /883B versions of the ADG201 can be purchased against the SMD 5962-B6716; The /883B version of ADG508ATO is described on DESC drawing 7705201EX . . . Six grades of the AD7537 12-bit monolithic dual M-DAC with on-board latches are now available against SMD 5962-87763 . . . /883B versions are now available for 2S80 monolithic resolver-to-digital converter, S & T grades . . . SMDs for instrumentation amplifiers: 5962-88539 for the AD524 and 5962-87719 for the AD625 . . . Now qualified to /883B: AD9002 8-bit, 125 MSPS flash a/d converter, AD629 analog trig-function IC, AD9610 wide-bandwidth fast-settling transconductance operational amplifier, AD96685 and AD96687 ECL comparators, and HTC-0300A track-and-hold amplifier.

PATENTS . . . 4,761,636 to A. Paul Brokaw and Modesto A. Maidique for A-to-D Converter of the Successive-Approximation Type . . . 4,769,564 to Douglas Garde for Sense Amplifier . . . 4,771,011 to Steven M. Hemmah and Richard S. Payne for Ion-Implanted Process for Forming IC Wafer with Buried-Zener Diode and IC Structure Made with Such Process . . . 4,774,685 to Howard R. Samuels for Approximation System.

IN THE LAST ISSUE

Volume 22, Number 1, 1988—36 Pages

Editor's Notes, Authors

Disk-Read ICs Condition and Deliver Bits at 50 Mbits/second (AD890, AD891)

Precision Bipolar Op Amp Has Lowest Offset, Drift (AD707)

a Low-Cost True-RMS Chips Also Compute AC-Average Response (AD7367)

True 18-Bit DAC in Hybrid Package Has Small Size, Low Cost (AD1139)

12-Bit A/D Converters for DSP Provide Complete Interface (AD132/133A)

Monolithic Digitally Programmable Delay—8-bits-to-Time Converter (AD9500)

15 New CMOS Switches and Multiplexers in Convenient Variety (ADG Series)

Fast Monolithic Log Amp with Better Than 250-MHz Bandwidth (AD9521)

Fast DSP Microprocessor: 1,024-Point Radix-4 FFT in 3.0 ms (ADSP-2100A)

CMOS Video DACs Provide Memory, Interface, and 3 Outputs (ADV471/478)

Monolithic 12-Bit Quad Voltage-Output Readback DAC (AD664)

Voltage-to-Current Isolator with High Accuracy (1B21)

AD652: Improved Monolithic Synchronous V/F Converter

12-Bit Monolithic CMOS ADC Guarantees 3- μ s Conversion Time (AD7672)

VMEbus Video Digitizer Boards to Match Your Source (RTI-683/684-HS)

Data-Acquisition and Control Software for PC Plug-Ins (Control EG-AC1904)

New Benchtop-Tester Enhancements Include High-Accuracy Op-Amp Board

New-Product Briefs:

8-MIPS Multibus II Array Processor Based on ADSP-2100 (RTI-980)

100-MHz 8-Bit Flash Converter is TTL-Compatible (AD9012)

Monolithic 8-Bit Video DAC has 250-MHz Update Rate (AD9701)

The AD9611 280-MHz Op Amp: 7-ns 1% Settling, Low Distortion

High-Speed TTL Comparator Has 7-ns Propagation Delay (AD9686)

Lowest-Cost Complete Voltage-Out 8-Bit DACPORT, +5-V Supply (AD557)

Isolated, Linearized Thermocouple Input Module: J, K, T, E, R, S, B (5B47)

12-Bit, 1-MHz Tracking ADC in a DIP: NMC Over Temp (AD9003)

Complete 15- μ s 12-Bit ADC, Pin Compatible with AD574A (AD674A)

Analog Devices Names 3 New Fellows: Jody Lapham, Bob Tsang, Mike Tuthill

More Authors

Worth Reading

Potpourri

Advertisement

FEATURES

10ps Delay Resolution
2.5ns to +100µs Full Scale Range
Differential Inputs
Separate Trigger and Reset Inputs
310mW Power Dissipation

APPLICATIONS

ATE
Pulse Deskewing
Phase Correction
High Stability Timing Circuits
Waveform Generators

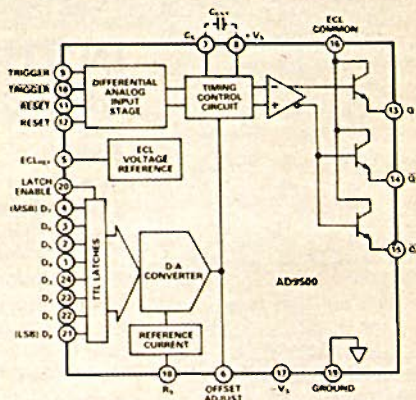
PRODUCT DESCRIPTION

The AD9500 is a digitally programmable delay generator which includes virtually all the circuits needed for generating time delays for digital pulses. It provides 256 programmed delays in a user-specified full scale range which can be varied from more than 100µs to as little as 2.5ns. On the latter scale, it can resolve increments as small as 10 picoseconds.

Its output is delayed from the input by a time which is directly proportional to the 8-bit digital input code. Using groups of AD9500 devices is an excellent way to adjust signal timing skews and delays in various system applications.

Differential TRIGGER and RESET control inputs are designed primarily for ECL signal levels but will also function with analog and TTL levels. An on-board ECL reference midpoint allows both to be driven by either single-ended or differential ECL circuits.

Two temperature ranges and three packages are available. For industrial temperatures of -25°C to +85°C, order the AD9500BP or the AD9500BQ. The "P" suffix indicates a 28-pin PLCC; the "Q" designates a 24-pin ceramic "skinny" DIP with 0.3" package width. For extended temperatures of -55°C to +125°C, order the AD9500TE (28-pin LCC) or AD9500TQ (24-pin "skinny" DIP).



AD9500 Functional Block Diagram

PRODUCT HIGHLIGHTS

1. The AD9500 delay generator is an extremely versatile but remarkable, easy-to-use timing device. A few basic configurations can be expanded and extended into multiple applications.
2. Accurate control of pulse timing is critical for all digital electronic systems, and many systems require that delays be controlled digitally. Until now, the majority of systems using that technique used discrete LSI devices which may consume up to one watt or more of power. The AD9500 performs the same function with 300mW of power.
3. Like a high speed counter, the AD9500 can be programmed with a binary digital word. This makes the unit a variable delay device, in effect, a digital-to-time converter (DTG). The digital input word scales the time reference of the AD9500 in essentially the same way a digital word scales voltage or current references in a DAC.

**TO SAVE HOURS
IN DIGITAL TIMING DESIGN, SPEND
A FEW MINUTES ON THIS PAGE.**



If you can't afford to spend hours designing and testing your own time delay circuits, then take a few minutes to learn about our new AD9500 monolithic time delay generator. It combines all the

functions you need to generate time delays for digital pulses on a single chip, so all you have to do is specify and order.

This unique, one-part solution also helps conserve board space and power, since the AD9500 is available in skinny 24-pin DIP or 28-pin LCC or PLCC packages, and dissipates only 310mW.

But its small size and low power consumption don't mean low performance. The AD9500 allows you to use an 8-bit TTL control word to select any one of 256 delay increments in a full-scale range of 100µs to 2.5ns. At the low end, you can resolve delays to 10ps.

And the AD9500 comes in the standard industrial temperature range of -25°C to +85°C, or an extended range of -55°C to +125°C.

In addition, the AD9500 is ECL compatible and usable with analog as well as TTL input levels. These features make it ideal for adjusting cable delays in multichannel ATE systems, or phase correction and timing generation in radar/ECM.

The AD9500 is not only quick to help you with your designs, it's quick to save you money, too. Prices start at \$16.00 each (in 100s).

With the AD9500, you won't have to waste another minute on time delay generation. So don't delay - call your nearest Analog Devices sales office, or our applications engineers at (919) 668-9511 soon.



Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 539-2037; Colorado: (719) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 251-9550; Austria: (222) 885504; Belgium: (3) 237 1672; Denmark: (2) 845890; France: (1) 4687-34-11; Holland: (1620) 81500; Israel: (052) 911415; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050

Use the reply card for technical data.